SONOMA STATE UNIVERSITY | ENGINEERING SCIENCE

Senior Design Project Progress Report
EE 492 Senior Design Project Planning

Adaptive Antenna Matching

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Acknowledgments

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Abstract

In this project, we are developing a device that automatically adjusts the antenna of wireless devices to improve the strength of their signal. The main goal is to make sure the antenna maintains its signal by triggering a change in its settings, when the environment around the device changes. An example of this is when a person is near the antenna or when it's near a wall. The way the device is able to keep the antenna performance is by pairing it up with a matching network, to adjust its impedance when it detects a change has occurred. The project aims to achieve optimal performance while also having low power consumption, minimal delay, and minimal insertion loss, this then results in a solution for applications that require wireless adaptive impedance matching.

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1. Problem Statement

The problem we are addressing with our adaptive antenna matching device is for manufacturers of wireless devices seeking to enhance the reliability of their products. Connectivity issues seem to be more prevalent when the antenna of a device encounters a change in its environment, such as when the device is placed near a person's body. This proximity changes the characteristics of the antenna itself, which can disrupt the signal and lead to an unstable connection. Additionally, when the antenna characteristics fluctuate, the device draws more power to compensate, which not only increases energy consumption, but also shortens the device's battery life. Ensuring a stable, reliable connection—regardless of usage conditions or environmental factors—is crucial for maintaining optimal device performance. Our solution aims to optimize the antenna's performance, enabling seamless connectivity while minimizing power consumption, thus extending the operational life and improving the reliability of wireless devices.

2. Introduction

As wireless technology becomes increasingly popular in consumer electronics, the demand for reliable, energy-efficient wireless devices has skyrocketed. However, wireless devices often face significant challenges when it comes to maintaining stable connectivity, especially in dynamic environments where the positioning and orientation of the device can vary. These challenges are especially apparent when the device's antenna interacts with its surroundings, such as when placed near a user's body. In such cases, the antenna's characteristics change which often leads to signal degradation, unstable connections, and increased power consumption. Moreover, as devices attempt to compensate for fluctuating antenna performance, battery life can be compromised, reducing the overall user experience. To address these issues, manufacturers need innovative solutions that help ensure consistent connectivity while optimizing power usage.

This project proposes an adaptive antenna matching device designed to enhance the performance and reliability of wireless wireless devices. By dynamically adjusting the antenna's impedance to match environmental changes, our solution minimizes signal disruptions, improves connection stability, and reduces power consumption. This not only extends battery life but also ensures continuous communication in a variety of usage scenarios. Our approach is crucial for manufacturers looking to deliver reliable wireless devices that maintain optimal performance, regardless of the user's environment.

3. Literature Review and Previous Works

In thinking about how to design our adaptive antenna matching device, we did some initial research on previous works aimed at addressing the challenges posed by unmatched circuits. This review explores the works and highlights some of the key findings as well as identifies gaps that our research aims to address.

One method we encountered is using a multiple circuit switching network. The process involves a microcontroller running an impedance-matching algorithm, which is connected to a directional coupler that measures forward and reverse (reflected) power levels. Based on these measurements, the microcontroller determines the optimal impedance match and uses relays to switch inductors and/or capacitors, which are aligned in an L, T, or Pi network, into the circuit to achieve the best matching and minimize the Standing Wave Ratio (SWR). This method has a few limitations. One limitation is that the matching network typically relies on a finite number of components, so the resolution may be limited by the number of relays and capacitors/inductors available. This could lead to less precise matching, especially for impedances that are close to the boundaries between the available settings. Another limitation is the tuning speed. The process of finding the optimal match may take up to a few seconds, which may not be fast enough for applications where the frequency or environment changes rapidly, such as in mobile use. While this method is effective for many applications, such as amateur (Ham) radio, where manual tuning is impractical, it may not be as suitable for other applications that demand more dynamic adjustments or faster response times. Additionally, factors like size, cost, and tuning speed may make these tuners less practical for applications requiring frequent or real-time impedance adjustments [1].

Another method employed was to use a digital circuit to control two varactors in a pi configuration. The way this method worked was to first measure the current value of mismatch using a directional coupler circuit. A switch was then turned on which increased the voltage to varactor VC1. The reflection measurement was then taken again immediately after the voltage was increased, and the value was compared to the last value of mismatch. If the mismatch increased, the switch was turned off, removing voltage to VC1. If the mismatch decreased, the switch was left on for a specific frame of time. During the frame of time, the VC2 varactor was held constant via a Sample and Hold circuit. After the specified frame of time had elapsed, voltage was applied to the VC2 varactor in a similar manner. A major advantage of this method is that it is fairly simple to implement and does not require complicated modeling or signal processing. Another advantage is that this method was able to improve mismatch by 4dB compared to a fixed capacitance matching circuit in simulation. The downside of this method is that there were no actual measurements taken; this is a purely theoretical method. As such, a lot of assumptions were made: the range of the antenna impedance moved only within the inductive half of the Smith chart, ideal operating conditions i.e no noise or interference from other devices or electronics, no fluctuations in frequency (used a fixed 2.54GHz), no temperature effects, etc. Additionally, no specifications were given about the power of the system, nor was an evaluation done to measure the insertion loss [2].

4. Methodology

We will approach the problem of antenna detuning due to the coupling of an object or body part placed near the antenna by developing an adaptive antenna matching device. This device will utilize a Software Defined Radio (SDR), an FT232H module, a microcontroller, two external digital to analog converters (DACs), a voltage translation circuit, and an adaptive pi matching network using varactor diodes. The FT232H module will be used to not only power the voltage translation circuit and external DACs, but also to interface the SDR and microcontroller. The varactor diodes will be reverse-biased and will be used to dynamically adjust the capacitance in the pi matching network. The system will utilize real-time feedback from the SDR to continuously monitor the antenna's performance, while the microcontroller will be running an adaptive algorithm to adjust the reverse voltage on the varactors to ensure the antenna operates at its best by minimizing reflections and maximizing power transfer. We will begin our project by building a frequency scaled version that operates around the 30-40 MHz range for testing and learning purposes. Once we have a thorough understanding of the objective, we will then scale the frequency up to be operable in the 1.8 GHz range.

Software Defined Radio (SDR) Integration:

We will be using a bladeRF 2.0 micro xA5. The SDR will be responsible for not only transmitting the 1.8GHz continuous wave RF signal, but also capturing any reflected signal from the directional coupler and analyzing the return loss (S11) or magnitude of the reflection coefficient. By continuously monitoring the impedance mismatch, the SDR will provide real-time data to the microcontroller on how well the antenna is matched to the rest of the RF system. This continuous monitoring ensures that any fluctuations or shifts in the antenna's performance are detected instantly.

Microcontroller for Real-Time Control:

Based on the feedback from the SDR, the microcontroller will issue instructions to the DACs which are responsible for outputting analog values corresponding to voltage levels for the varactors. The microcontroller we will be using will be a PIC18F47K42 via the Curiosity Nano module. It will receive the real-time measurements of the antenna's reflection or mismatch from the SDR and will make immediate adjustments to the matching network, ensuring minimal signal loss.

Voltage Translation Circuit:

The voltage translation circuit will be powered via the 5V supply of the FT232H module. The voltage translation circuit will be used to boost the source voltage of the FT232H module output up to 15V DC. This high voltage will be used to operate an LM358AN operational amplifier (op amp) that is used to amplify the signals coming from the DACs. These signals will then be used to vary the voltages to the varactor diodes which in turn vary the capacitance of the diodes in the matching network.

Adaptive Matching Network with Varactor Diodes:

The matching network, which includes two varactor diodes and an inductor in a pi configuration, will be key to dynamically adjusting the impedance of the antenna. The varactor diodes we will be using will be two Skyworks SMV1276-079LF varactors and a fixed 2.2nH inductor which

will be controlled by the microcontroller. These diodes enable fine-tuned adjustments to the impedance without the need for manual tuning, which is crucial for real-time adaptability.

5. Challenges and Risks

In our project focused on developing an adaptive impedance matching circuit, we have identified and assessed several risks that could impact the success and efficiency of the system. This report outlines these risks, their qualitative scores, and our strategies for mitigation and contingency planning, as summarized in the table.

5.1 Damage to components during testing

Since testing components for high-frequency matching often involves delicate adjustments and high voltages, there is a significant risk of component failure.

Risk Score:

High (Likelihood = 2, Consequence = 4, Total = 8)

Mitigation Plan:

We will conduct thorough simulations and perform detailed calculations before physical testing. This approach minimizes the likelihood of unexpected electrical stress on components.

Contingency Plan:

Recognizing that some failures may occur, we will order extra components as part of our initial order to ensure replacements are readily available, minimizing delays.

5.2 Inability to meet project time constraints

Due to the complexity of adaptive impedance matching, which requires precise tuning and calibration, time management is crucial. We may run into unforeseen challenges that require more of our time and attention than anticipated.

Risk Score:

Extreme (Likelihood = 4, Consequence = 4, Total = 16)

Mitigation Plan:

A clear project schedule with milestones and deadlines will be established to maintain steady progress. We will also initiate simulation and testing activities at the earliest stages. Early testing helps identify potential design flaws sooner, allowing for timely adjustments.

Contingency Plan:
If delays occur, the schedule will facilitate prioritization of critical tasks to ensure core functionality is achieved on time.

5.3 Unpredictable behavior at 1.8 GHz

At 1.8 GHz, the performance of RF components can be impacted by the resonant frequency of the components, as well as parasitic inductance and capacitance.
Risk Score:
Extreme (Likelihood = 4, Consequence = 4, Total = 16)

Mitigation Plan:
We will select low-parasitic components, optimize PCB layout, and perform extensive testing to confirm the system's behavior at high frequencies, adjusting component values or trace routing as needed.

Contingency Plan:
If unpredictable behavior is detected, we will perform a detailed analysis to identify the specific components or areas of the circuit causing the issue. We may replace problematic components with alternatives designed for better high-frequency performance and/or redesign affected portions of the circuit

5.4 Creating a fast, adaptive algorithm.

The real-time adaptive response of the system may be delayed due to system latency, particularly when the algorithm is complex.
Risk Score:
High (Likelihood = 4, Consequence = 4, Total = 16)

Mitigation Plan:
We have chosen a microcontroller with a clock speed capable of meeting our projected response time requirement. We will thoroughly test the algorithm in simulation while also simplifying it as much as possible.

Contingency Plan:
If the response time falls outside our target range, we will revise the algorithm or explore further simplification. Additionally, we will evaluate alternative microcontrollers that can execute the required operations more efficiently.

5.5 System losses are greater than what is saved

The use of certain components or configurations in the antenna matching network may result in greater system losses than initially anticipated, negating the benefits gained from adaptive matching.

Risk Score:

High (Likelihood = 3, Consequence = 4, Total = 12)

Mitigation Plan:

Test directional coupler directly and in series with the matching network.

Contingency Plan:

Purchase a higher-quality directional coupler.

5.6 Device Power Consumption Exceeding Ideal Levels

High power consumption can compromise the efficiency and performance of the impedance matching circuit.

Risk Score:

High (Likelihood = 2, Consequence = 3, Total = 6)

Mitigation Plan:

We will implement low-power components, ensuring that the device consumes a reasonable amount of power relative to its intended purpose and functionality.

Contingency Plan:

If power consumption remains high, we will refine the system design to optimize power usage further. This may involve selecting more energy-efficient components or optimizing the circuit layout to help reduce losses.

Summary:

This risk assessment and management plan is critical to the successful execution of our adaptive impedance matching circuit project. By addressing these concerns, we aim to mitigate the primary risks associated with high-frequency adaptive circuit design. With proactive simulation, careful scheduling, and a focus on power efficiency, we are well-positioned to overcome these challenges and achieve our project goals.

6. Project Requirements

Projects have two requirements to help guide their development, marketing and engineering requirements. Marketing requirements are the requirements that are important to the customer while engineering requirements are the requirements that are practical from an engineering perspective.

6.1. Marketing Requirements (MR)

MR-1. The device shall continuously adapt to changes in the impedance of the antenna.

MR-2. The device shall not consume a significant amount of power to operate.

MR-3. The device shall have no user intervention for adaptive feature to operate.

MR-4. The device shall respond to changes in impedance with minimal delay.

MR-5. The device shall operate within the center of the wireless frequency range.

MR-6. The device shall not create more insertion loss in the RF path than what is saved.

6.2. Engineering Requirements (ER)

ER-1. The device must be able to match a load impedance with a starting VSWR of 2.0 or less to within a VSWR of 1.22 ($\geq$ 20 dB return loss). **(MR1)**

ER-2. The device must have a power consumption of less than 700 mW during operation. **(MR2)**

ER-3. The device must be able to make adjustments autonomously when in operation. **(MR3)**

ER-4. The device must respond to changes in impedance within 100 ms to ensure minimal delay in performance. **(MR4)**

ER-5. The device must operate effectively at a frequency of 1.8 GHz. **(MR5)**

ER-6. The insertion loss of the matching network should be less than 2 dB. **(MR6)**

7. Implementation

The implementation of the adaptive antenna matching device will be carried out in several stages, each focusing on a specific aspect of the project. The stages include hardware setup, software development, system integration, and testing. The first phase of the project will focus on building a frequency scaled test setup for practicing antenna matching using a pi matching network with varactor diodes and a Keysight FieldFox for measurements. The purpose of this phase is to gain hands-on experience with adjusting the antenna impedance to minimize reflection and ensure optimal signal transmission. The Software Defined Radio (SDR) and microcontroller will not be involved in this phase, as the goal is to focus on manual or basic controlled adjustments to the matching network. This will help us in developing our algorithm

for adaptive adjustments. The second phase involves scaling the frequency up to the wireless frequency range of 1.8 GHz. In this phase, we will introduce the SDR, the microcontroller, and a voltage translation circuit to operate the varactors in addition to our pi matching network, directional coupler and antenna. This will be our final product.

7.1. System Architecture of Frequency Scaled Model

The initial phase involved constructing a simplified setup featuring a pi-matching network and arbitrary loads. This setup, operating at 30-40 MHz, served as a frequency-scaled prototype of the final product. It was used to refine impedance matching techniques by adjusting the capacitance of varactor diodes using a DC power supply as well as in developing our impedance matching algorithm.

Hardware Setup: (see testing section for schematics)

A pi matching network was constructed using two NTE614 varactor diodes and a 171 nH inductor. The network was designed to match the impedance of the arbitrary loads. The arbitrary loads simulated the target impedance to practice adjusting the matching network. The loads spanned different impedances to test the network's performance under various conditions. A FieldFox was used to provide real-time data on the performance of the matching network as the varactor diodes' capacitance was adjusted. A DC power supply was used to vary the reverse voltage on the varactor diodes, adjusting their capacitance and enabling tuning of the matching network.

Software Setup:

The FieldFox was first calibrated to establish the calibration plane. This ensures that any port extension is accounted for, allowing for accurate measurements. It was then configured to output a 30-40 MHz signal as well as to measure the return loss (S11) or magnitude of the reflection coefficient. It displayed real-time data showing how well the antenna was matched to the rest of the RF system as the varactors in the pi network were adjusted.

System Integration:

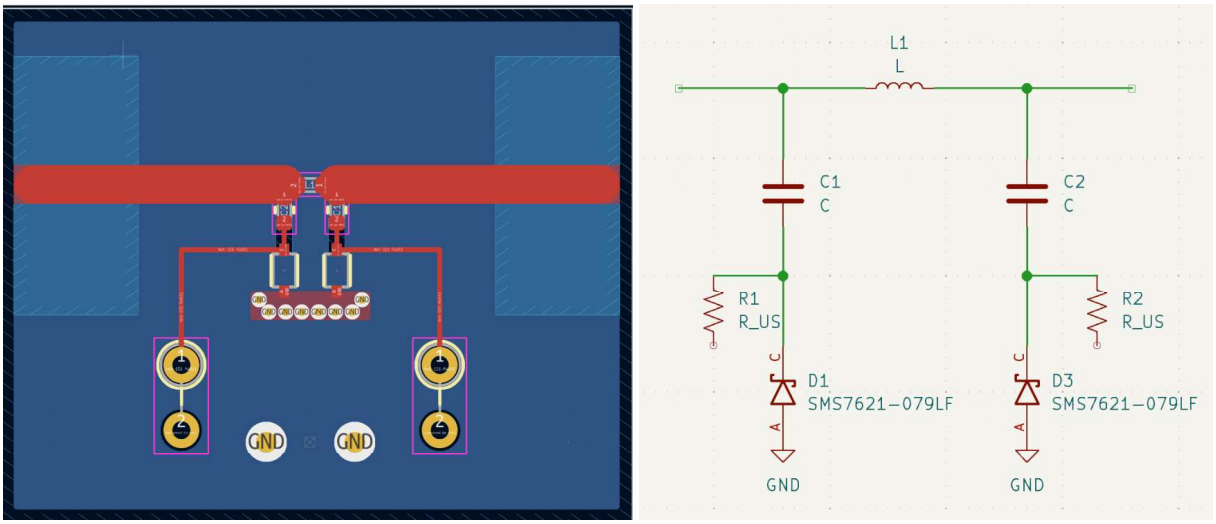
The FieldFox captured real-time data of the reflected signal, which served as the feedback for our system. The FieldFox monitored the reflection while the matching network was manually adjusted using a DC power supply. The goal was to reduce the return loss as much as possible, signaling that the impedance was matched properly.

7.2. System Architecture of 1.8GHz model

Now that we have successfully validated the system in the 30-40 MHz range, the matching network setup will be scaled to the 1.8 GHz wireless frequency range. During this phase of our project, the SDR and microcontroller are introduced along with a voltage translation circuit to operate the varactors.

Hardware Setup:

The matching network consists of a 1.8nH inductor and two SMV1276-079LF varactor diodes in a PI topology. The schematic and PCB layout are displayed below.



Since the varactors will require 1.5-10V, we have introduced a voltage translation circuit. This circuit consists of a boost converter module which takes in +5V and outputs +15V used to power an LM358AN dual op amp circuit. The boost converter module itself is made up of an MT3806 IC (integrated circuit) chip that ultimately works as a switch, a 22µH inductor which is used to store the energy needed to boost the voltage from +5V to +15V, a SS34 Schottky diode used to prevent current from flowing back toward the source while the switch is closed while allowing current to flow and charge a capacitor while the switch is open. Additionally, there are some filtering capacitors and feedback resistors which are used to set the desired output voltage. The op amp circuit uses four resistors, one 22kΩ and 10kΩ for each op amp, to produce a gain of 3.2V/V, as well as some filtering capacitors.

The DACs used were two MCP4725 modules. These are 12 bit resolution DACs capable of outputting 4095 different voltage values. Each DAC can be configured to operate at 100kHz, 400kHz, or 3.4MHz. 100kHz was selected as a starting point, but later configured using 125kHz. Two 10kΩ pull-up resistors were used on the SDA (data) and SCL (clock) lines for each DAC. Additionally, several filtering capacitors and low pass filters were used.

A BladeRF Software Defined Radio (SDR) is used to essentially operate as a one-port network analyzer. A MAC Technology directional coupler is connected to the TX port of the SDR while

the reflected power port of the coupler is connected to the RX port. The matching network then sits between the through port of the coupler and the antenna.

Software Setup:

The bladeRF was configured to output values every 3.4milliseconds. This is the fastest that Gnuradio allows in order to be able to work properly with the microcontroller (more details on this later).

The PIC18F47K42 microcontroller is used to execute the algorithm used for matching as well as to operate the DACs using I^2C communication protocol. MPLAB X IDE v.6.20 was used to program the DACs as well as to configure the algorithm used for our adaptive antenna matching. The algorithm consists of …….(more to come).

System Integration:

The SDR will be responsible for producing a 1.8GHz continuous wave signal that will then be transmitted through the antenna. Any reflection from the antenna will be received from the SDR via the directional couplers' reflected signal port and processed in Gnuradio's Python block. The value will be sent through the FT232H to the PIC, which then sends new voltage values to the varactors via the DACs if the antenna is not matched.

7.3. Alternative Design Matrix

Utilizing design matrices allows us to identify components that fulfill our project requirements effectively. This process involved a thorough examination of datasheets to extract and evaluate the performance metrics of each component against the established criteria. Below are the design matrices for some of our major components:

Table 7.3.1 Microcontroller design matrix

Criteria	Weight	ESP32	PIC18F47K42	ATmega328	STM32F103C8T6
Power Consumption (mA)	0.45	0.13 (40)	0.28 (18.6)	0.38 (14)	0.21 (25)
Time to Market	0.3	0.14	0.51	0.21	0.14
Price ($)	0.1	0.29 ($3.00)	0.25 ($3.48)	0.32 ($2.63)	0.14 ($6.11)
Clock Speed (MHz)	0.1	0.61 (240)	0.16 (64)	0.04 (16)	0.19 (72)
Memory (RAM Kb)	0.05	0.91 (320)	0.02 (8)	0.01 (2)	0.06 (20)
Score		0.24	0.32	0.27	0.17

Table 7.3.2 Directional coupler design matrix

Criteria	Weight	BDCA-10-25+	BDCA1-10-40+	BDCA-15-25+	BDCA-7-25+

Return Loss (dB)	0.35	0.30 (25)	0.28 (23)	0.22 (18)	0.20 (17)
Insertion Loss (dB)	0.25	0.25 (1)	0.24 (1.03)	0.35 (0.7)	0.16 (1.6)
Coupling Loss (dB)	0.2	0.26 (10)	0.23 (9.1)	0.33 (13)	0.18 (7)
Directivity (dB)	0.2	0.30 (23)	0.30 (23)	0.19 (15)	0.21 (17)
Score		0.28	0.26	0.27	0.19

Table 7.3.3 Varactor diode design matrix

Criteria	Weight	Skyworks SMV1276-079LF	SMV1233	SMV2019	SMV1405
Capacitance Range (pF)	0.6	0.41 (5.63)	0.31 (4.24)	0.14 (1.92)	0.14 (2.04)
Tuning Voltage Range (v)	0.3	0.29 (16)	0.31 (15)	0.24 (20)	0.16 (30)
Price ($)	0.1	0.23 (0.85)	0.12 (1.68)	0.42 (0.48)	0.23 (0.85)
Score		0.36	0.29	0.19	0.16

Table 7.3.4 Antenna design matrix

Criteria	Weight	W1030	GW.11.A153 W	343-ANT-W63WS4-SM A-ND	X1005800-W5DRMB
Return Loss (dB)	0.4	0.16 (-10)	0.16 (-10)	0.41 (-25)	0.27 (-16)
VSWR	0.3	0.18 (2)	0.35 (1)	0.30 (1.2)	0.17 (2.1)
Efficiency	0.15	0.25 (82)	0.24 (80)	0.24 (80)	0.27 (85)
Price ($)	0.15	0.41 (5.15)	0.21 (10.03)	0.28 (7.73)	0.10 (20.64)
Score		0.22	0.24	0.33	0.21

7.4. Budget/Parts List

Table 1 Description and list of required components including their price.

Part/ Quantity	Price	Description	Link	Test	ER#
Microcontroller (PIC18F47K42)/ 1	$3.48	MCU for processing impedance adjustments and controlling matching network	https://www.digikey.com/en/products/detail/microchip-technology/PIC18F47K42-I-P/8536645	FT.2, ST.1	ER3

PICKIT3 Programmer/ 1	$31.99	In-circuit debugger and programmer for the PIC18F47K42 microcontroller.	https://a.co/d/46WeLkz	FT.2, ST.3	ER3
Directional Coupler / 1	$9.02	Measures reflected and forward power, allowing impedance matching calculations	https://shorturl.at/OWoLO	FT.3	ER1, ER4
Varactor Diode / 2	$3.36	Variable capacitance diode to adjust impedance matching	https://www.digikey.com/en/products/detail/skyworks-solutions-inc/SMV1235-079LF/2408395	FT.3, ST.3	ER1, ER4
Antenna / 1	$7.73	Transmits and receives signals, to adjustment for impedance	https://www.digikey.com/en/products/detail/te-connectivity-linx/ANT-W63WS4-SMA/16511113	ST.3	ER1, ER5
Adafruit FT232H Breakout / 1	$14.95	USB to serial converter for communication	https://www.adafruit.com/product/2264	All	ER3, ER4
Boost Module / 1	$5.99	Boost converter for power regulation	https://shorturl.at/r0gp7	All	ER3, ER4
DAC Breakout Module / 1	$2.98	Digital-to-analog converter for signal processing	https://shorturl.at/yAGIt	All	ER3, ER4
PCB Board and Assembly / 1	$60.00	Custom circuit board to integrate components	https://www.pcbway.com/pcb-assembly.html	All	All

Misc. Passive Components (Resistors, Capacitors, Inductors) / Set	$15.00	Additional components for impedance matching network	https://www.digikey.com/	FT.3	ER1
Total Cost	$154.50				

7.5. Project Schedule

We used some of last year's Gantt charts as examples to build our Gantt chart/schedule. Even though we are all working closely together on the entire project, we have divided up some of the tasks according to who is responsible for taking the lead on that task. This schedule covers the time frame from the month of November to May when the Spring semester is officially over. Additionally, this schedule may be subject to change as the project progresses through its different stages. In the event that there are changes to the schedule due to unforeseen challenges or problems encountered, the schedule will be adjusted accordingly.

Table 2 Gantt Chart / Schedule for Fall and Spring Semesters

8. List of Tests (Must include 5-10 major tests)

We divide this section into Functional Tests (FT) and System Verification Tests (ST). Functional Tests are defined as single component/module tests that verify Engineering Requirements (ER) of Project Requirements (section 6). System Verification Tests are defined as overall performance of system tests that validate the Marketing Requirements (MR) of our Project Requirements (section 6).

8.1. Summary of Tests

Below, we present a summary of tests that are planned to be performed. This list will be updated as testing progresses.

8.1. **Table 3** Summary of conducted tests.

Test Number	Objective	ER to address	Notes
FT.1	Testing of the antenna	ER.1	Complete
FT.2	Measure the Self-Resonant Frequency	ER.1, ER.3, ER.5	Complete
FT.3	Testing of the matching network for maximum VSWR	ER.1, ER.3, ER.5	Complete
FT.4	Testing the DACs	ER.2, ER.3, ER.4	Complete
FT.5	Test that voltage translation circuit for varactors operates properly	ER.2	Complete
FT.6	Test microcontroller algorithm	ER.1, ER.3	Complete
FT.7	Testing SDR can measure	ER.1, ER.5	Complete

	return loss		
ST.1	Measure the device's power consumption over a period of time	MR.2	Complete
ST.2	Determine how long the device takes to match an impedance	MR.4	Complete

8.2. Description of Tests

Testing of the Antenna:

Purpose:

We tested an antenna to evaluate the impact of hand movements—such as waving, wrapping, or repositioning—on the antenna's performance. This helped us determine the extent of performance degradation and provided insight into the required capacitance and inductance ranges for our matching network.

Setup:

For this test, we mounted the antenna on the FieldFox's S11 port. We then performed multiple hand movements while taking a video recording of the FieldFox's window results for a later analysis. The points were plotted on an online Smith Chart tool to view the range of impedances.

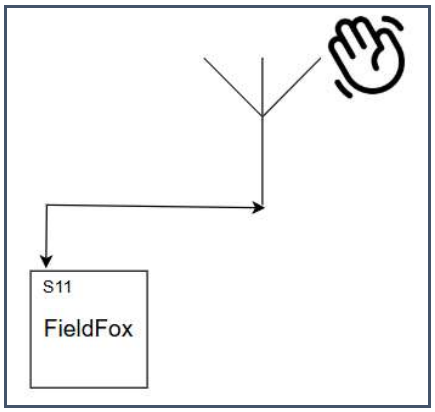


Figure 2: Circuit used for antenna testing.

Figure 3: Testing our antenna. Viewing the S11 parameter change on Keysight FieldFox as hand movements were made.

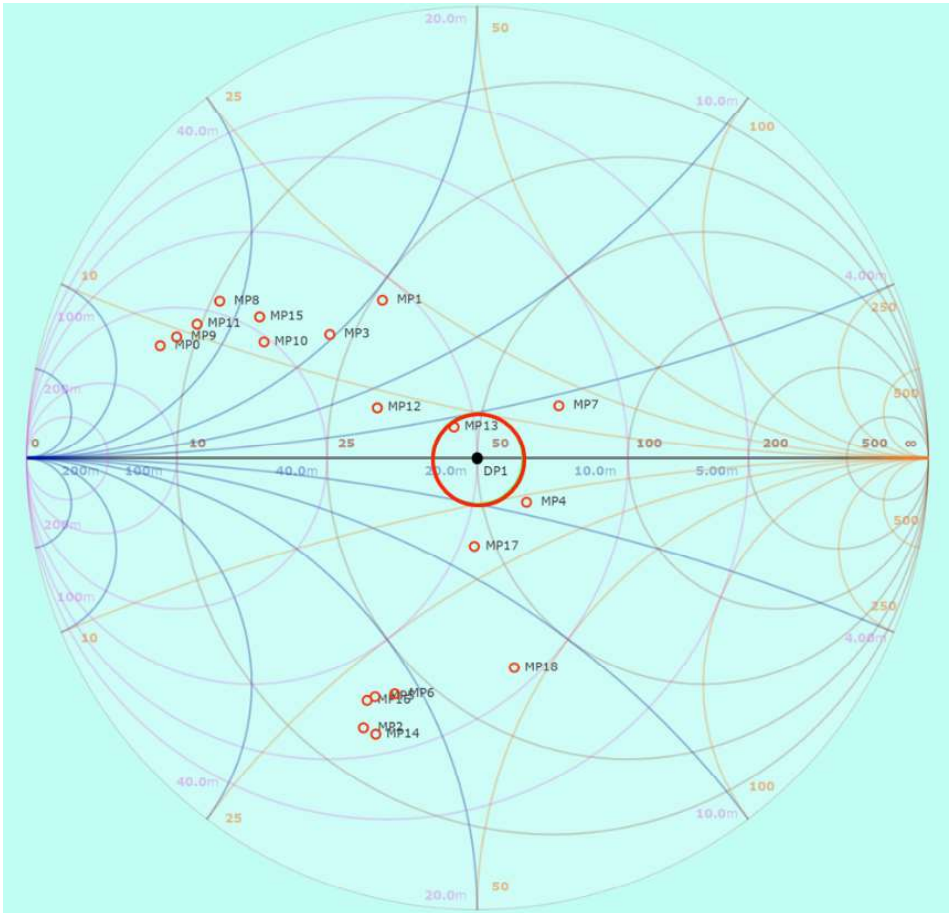


Figure 4: Plotting all the points identified from the Keysight FieldFox video on an online Smith Chart tool. The red circle and anything enclosed within it represents the target of >=20dB return loss.

- Results: The 1.8GHz antenna is quite poorly matched and highly affected by environmental changes. This is actually ideal as it presents an opportunity for our matching network and algorithm to demonstrate their efficacy.

- Proof of Concept:

- Requirements Satisfied: (ER.1)

Resonant Frequency:

Purpose:

Given that our system will be required to match impedances at frequencies in the 1.8 GHz range, we must carefully consider the behavior of the reactive components (varactor diodes and inductor) at such high frequencies to ensure that they behave as expected.

Setup: The first step will be to use existing SPICE model information to simulate the behavior of each component at the desired frequency. Upon successful completion, a vector network analyzer can be used to plot the resulting phase for a wide span of frequencies on a smith chart to determine at what point self-resonance occurs. The components under test can be soldered to a PERF board which will assume the role of the load. A single port connection to a VNA will be sufficient to plot the phase shifts as a function of frequency.

- Results: The SMV1276-079LF varactor diode, as demonstrated in simulation, achieves self-resonance at around 2.28GHz (assuming no reverse bias voltage). Given that our target frequency is 1.8GHz, we do not expect this to be problematic.
- Proof of Concept: The components under test will pass the test if and only if they show no signs of self-resonance up to at least 2.0GHz.
- Requirements Satisfied: (ER.1, ER.3, ER.5)

Testing of the Matching Network for maximum VSWR:

Purpose:

Our purpose is to adaptively match the impedance of the load to the source. Since it is not feasible to create a perfect match in all scenarios, we must decide on a maximum allowable VSWR (which in turn dictates the return loss), which will be heavily influenced by the algorithm employed by the controlling unit as well as our choice of capacitors and inductor. The purpose of this test will be to ensure that the algorithm(s) used can achieve a match to within a VSWR of no greater than 1.22dB (20dB of return loss) given an initial impedance that falls on or within a VSWR of 2.0 (about 9.4dB of return loss). This test will also help us gain a better understanding of how to develop our algorithm given that we will not be able to rely on phase information.

Setup:

This setup will involve a “scaled-down” version of a matching network to include components of much larger sizes, allowing for frequencies of around 10-30 MHz to be used. A transmission line will be terminated in an arbitrary load originating from the matching network. A member from our team will then gradually adjust the voltages across the varactor diodes while another monitors the return loss.

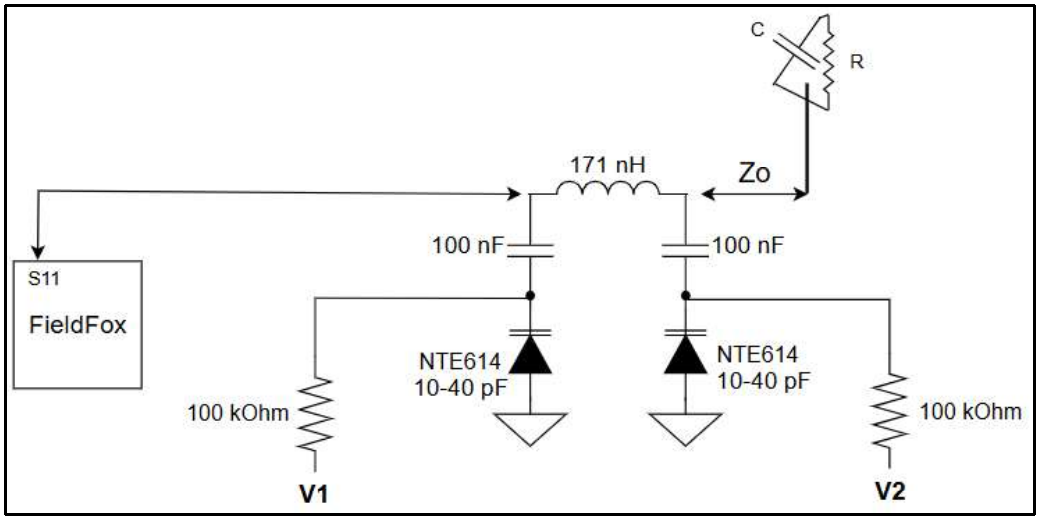


Figure 5: This is our circuit for testing the frequency-scaled matching network.

Figure 6: Arbitrary loads created to practice impedance matching and develop our algorithm.

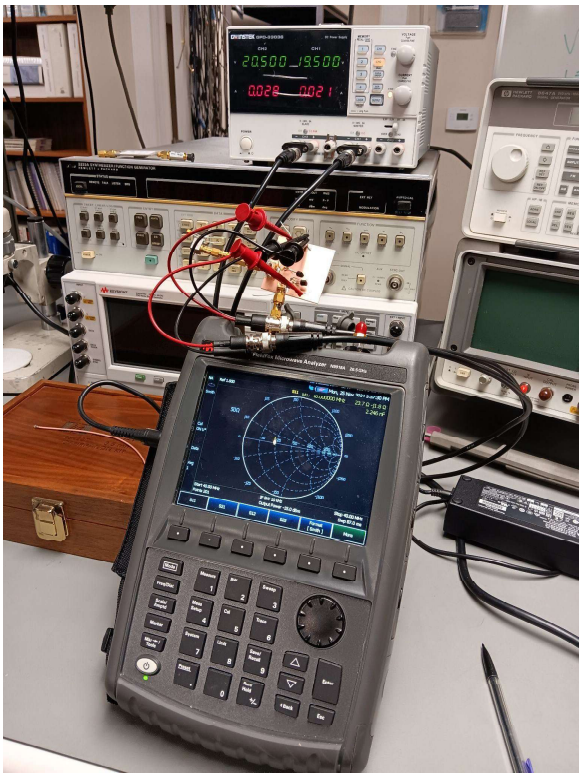


Figure 7: Testing the matching network with an arbitrary load. Here varactor 1 is set to a reverse voltage of 19.5 V, while varactor 2 is set to a reverse voltage of 20.5 V.

Figure 8: This was our matching network with an unmatched arbitrary load at 40 MHz.

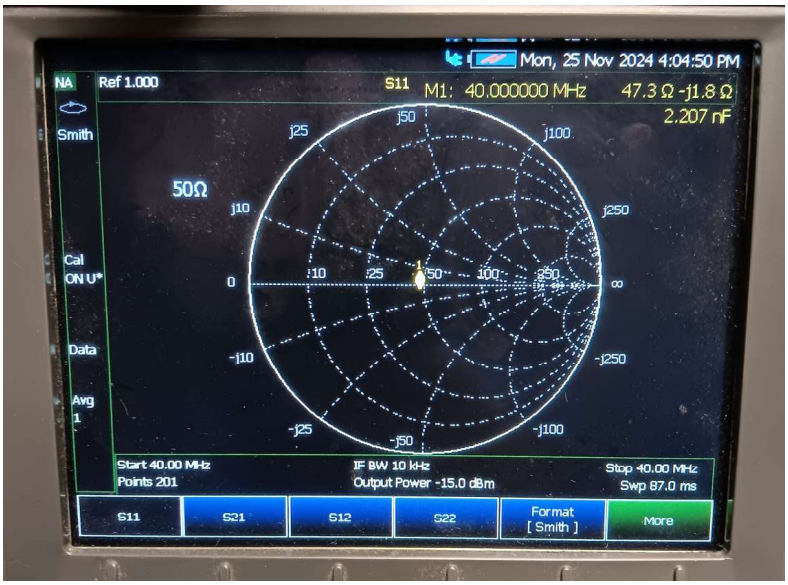


Figure 9: This was our matching network after manually adjusting the varactor reverse voltages. The impedance was almost perfectly matched.

- Results: The test was able to satisfy our requirement given the above constraints, albeit with mixed results and some unexpected behavior. We found that for loads on the left half of the smith chart (resembling more of a short circuit), whether capacitive or inductive, responded well to the matching network and were more than capable of being matched to within a VSWR of 1.22. Unfortunately, the same cannot be said for loads appearing to be more open, as these generally could not be matched to any better than a VSWR of 1.43.
- Proof of Concept: Despite promising simulation results, our scaled-version matching network could not perform as we had hoped in all scenarios. Nonetheless, it did show some promise as all four loads showed significantly improved return losses, even if the final impedances for all of them did not fall on or within a VSWR of 1.22.
- Requirements Satisfied: (ER.1, ER.3)

Testing the PCB

Purpose:

In high-frequency PCB design, special considerations must be taken to minimize the effects of stray reactances, which can degrade signal integrity and overall circuit performance. One key strategy is the use of multiple ground vias to reduce inductive impedance and ensure a low-impedance path to ground, which is especially critical for high-speed or sensitive analog circuits. Additionally, careful attention to ground plane clearances helps prevent unwanted parasitic capacitance and coupling between signal traces and other conductive elements. Tightly spaced components with overlapping courtyards may save board space, but they can also

introduce mutual inductance and thermal issues; thus, precise placement and routing are essential to avoid unintended interactions and maintain electromagnetic compatibility.

Setup:
After soldering the components onto the PCB, a bench supply was used to bias each varactor individually. The matching network was attached to the field fox on one end, and to a 1.8 GHz antenna on the other.

Results:
The matching network performed well overall for a variety of loads, in many cases exceeding out engineering requirements in two ways - firstly by increasing the return loss to well above 20dB (in some cases as high as 40+dB), and secondly by having a much greater tuning range by matching loads that began well outside a VSWR of 2.0 - the highest initial VSWR that was able to be matched was 3.43. This showcases the flexibility and robustness of our matching network design.

Testing the DACs:
Purpose:
Both the PIC18F47K42 datasheet and MCP4725 datasheet were used extensively in addition to a technical bulletin found on Microchip's website (see references [8], [9] & [10] for links) when programming the board/DACs. Unfortunately, the simulator on MPLAB did not work for testing and/or debugging, as the hardware handles most of the communication processes once the I^2C registers are configured properly and the appropriate flags are utilized. As a result, if one attempts to use the simulator, the code will hang in sections that the hardware handles without the ability to proceed (i.e. while loops). The purpose of this test was to ensure that the expected or needed voltage values for the varactors could be achieved at the outputs of the DACs.

Setup:
To carry out this test, it was important to first break it down into small steps of progression as follows:

Step 1: working with only outputting one value for one DAC

Step 2: working with outputting one value for the other DAC

Step 3: combining both DACs while outputting one value

Step 4: outputting multiple values on one DAC

Step 5: outputting multiple values on both DACs.

The setup is very similar for all steps:

The PIC18F47K42 Curiosity Nano Evaluation Kit board was used and connected via USB to a PC which is using MPLAB X IDE v6.20 with the XC8 v2.50 compiler. The regulated output voltage from the board is 3.3V; this value was used to power the DACs which are able to operate within a 2.7V to 5.5V supply. Although, when the 5V supply was used instead of the 3.3V, the DACs did not operate properly; therefore, a voltage of 3.3V was used. One thing to note is that the device's address consists of a device code nibble (1100), which is the same no matter what mode it is being operated in, followed by three bits (A2, A1, A0) and a read/write bit. Bits A2 and A1 are programmed as 0 from the manufacturer, while A0 could be either tied to GND (logic 0) or VCC (logic 1) via the solder pads on the front.

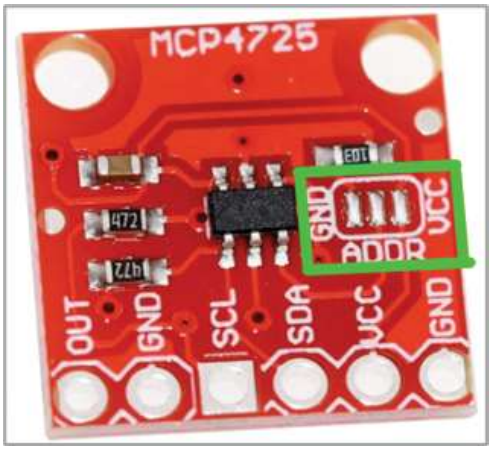


Figure.10 MCP4725 external DAC module. Highlighted are the solder pads used for configuring the device address.

For our setup, A0 was tied to GND for both DACs. As the DACs are operating on independent buses, this does not cause a conflict with both boards having the same address. Following the address byte, a user must configure the DACs based on their intended use with the second byte. Since the PIC18F47K42 is configured to operate at a frequency of 100kHz, the MCP4725 must match this frequency; therefore, this byte is set to a hex value of 0x40. The third byte consists of data bits D11-D4, while the second byte consists of data bits D3-D0 followed by 4 unused bits (logic 0). It is important to note that bytes 2-4 must be repeated in software.

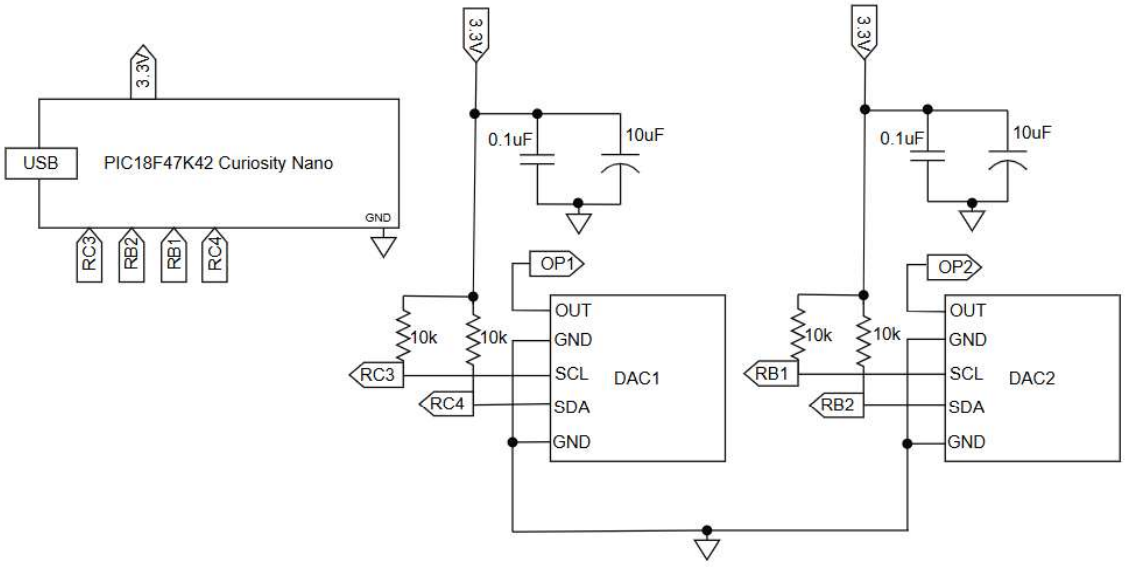


Figure: 11: Circuit diagram of testing the DACs. OP1 and OP2 are the DAC outputs used as inputs to the op amps.

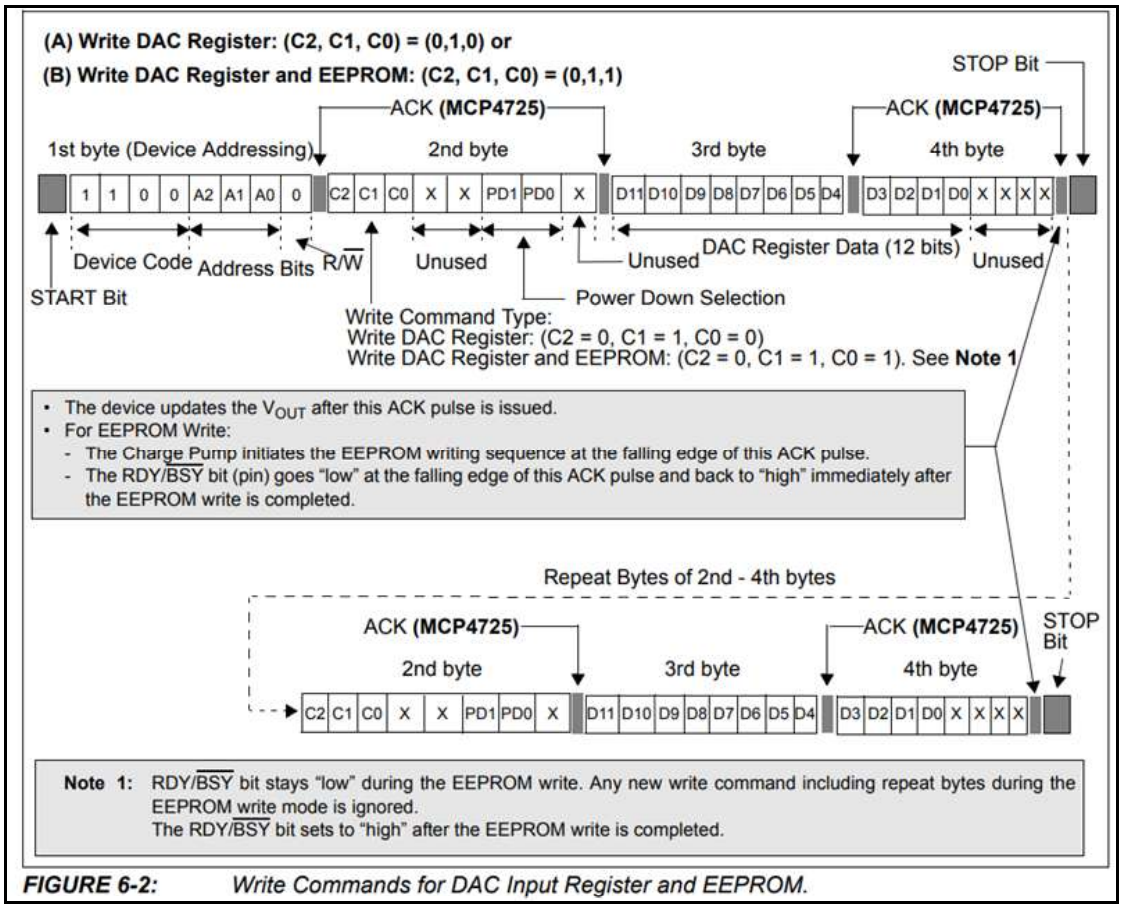


Figure. 12: MCP4725 data byte configuration process.

For Steps 1-3, the only tools used to ensure the code was operating correctly were debugging LEDs and a multimeter which made the task more difficult than expected, but it was accomplished nonetheless. LEDs were placed in different sections of the code to check for operation and/or errors. For Steps 4-5, a four-channel oscilloscope was introduced and used to view the different signals (clock, data, output1, output2); this tremendously helped with debugging and taking measurements.

In order to calculate the digital value needed, the given formula was used:

$$\# = \frac{Vout\,(2^n - 1)}{Vin}$$

Where '#' is the value needed to write to the DAC (rounded to the nearest whole number) in order to obtain the 'Vout' value. 'n' is the resolution of each DAC (12 in this case). 'Vin' is 3.3V as this was the value measured at Vcc.

Both DACs were able to output values within 2mV of theoretical value for this initial test.

Vr	Vin (op amp)	DAC # for 3.3V	DAC1 (A)	DAC2 (gold)	% Error DAC1	% Error DAC2
1.5	0.475	589	0.477	0.476	0.42	0.21
1.75	0.554	687	0.555	0.554	0.18	0.00
2	0.633	785	0.634	0.632	0.16	0.16
2.25	0.712	884	0.713	0.711	0.14	0.14
2.5	0.791	982	0.792	0.791	0.13	0.00
3	0.949	1178	0.951	0.951	0.21	0.21
3.5	1.108	1374	1.106	1.108	0.18	0.00
4	1.266	1571	1.265	1.266	0.08	0.00
4.5	1.424	1767	1.424	1.423	0.00	0.07
5	1.582	1963	1.582	1.581	0.00	0.06
5.5	1.741	2160	1.743	1.74	0.11	0.06
6	1.899	2356	1.902	1.898	0.16	0.05
7	2.215	2749	2.219	2.217	0.18	0.09
8	2.532	3142	2.536	2.533	0.16	0.04
9	2.848	3534	2.851	2.848	0.11	0.00
10	3.165	3927	3.168	3.164	0.09	0.03

Figure 13: The first column is the voltage needed at each varactor. The second column is the value needed at the input of each op amp of the voltage translation circuit in order to obtain the value in the first column. The third column is the value needed to write to each DAC to obtain the value in the second column. The fourth and fifth columns are the measured voltage values at the output of each DAC. Each DAC was given a label, as ten DACs were obtained, and each was tested for accuracy. The final columns are the percent errors of each DAC from expected value.

Figure 14: Oscilloscope results of testing the DACs. The yellow waveform is the SCL (clock) line of DAC1, the pink waveform is the SDA (data) line of DAC1, the blue waveform is the output OP1, the green waveform is the output OP2. Note: the points where the data line is pulled to zero are the ACKs (acknowledgments sent from the client to the host).

Figure 15: Same results as in figure 14. The cursors here are used to measure the delay between both outputs OP1 and OP2.

- Results: One of the difficulties encountered was determining which processes were handled by the hardware and which processes were to be handled by software. The datasheets were not clear on this. It has been found that when the ADB bit of the I2CxCON2 register is set (where x could be either 1 or 2) which is mistakenly labeled as 'ABD' in the datasheet several times, it is only necessary to write to the I2CxCNT register (which holds the number of bytes to be transmitted) and the I2CxTXB register (which handles the transmission of the data). One thing the datasheet never mentions is that the number of bytes to be transmitted does NOT include the address byte. The hardware seems to handle almost everything; the only thing software needs to do is probe the corresponding flags for each process, such as the Start, Stop, and BFRE (bus free) which add the necessary delays allowing the processes to finish. Additionally, the I2CxPIR flags must be cleared in software after each iteration.

  From figures 14 and 15, one can see that each value is held for 1.30mS. It also appears the outputs are offset by 650µS, which also means the values are the same value for only 650µS of the time. This should be taken into consideration in our algorithm.

  UPDATE: After testing for time response from the DACs, the idea of operating the DACs in "Fast Mode" became more desirable. The I^2C was reconfigured in MPLAB to reflect this mode of operation. However, the max I^2C clock speed that could be achieved was 125kHz. Making this change reduced the number of bytes being sent from 7 to 5.

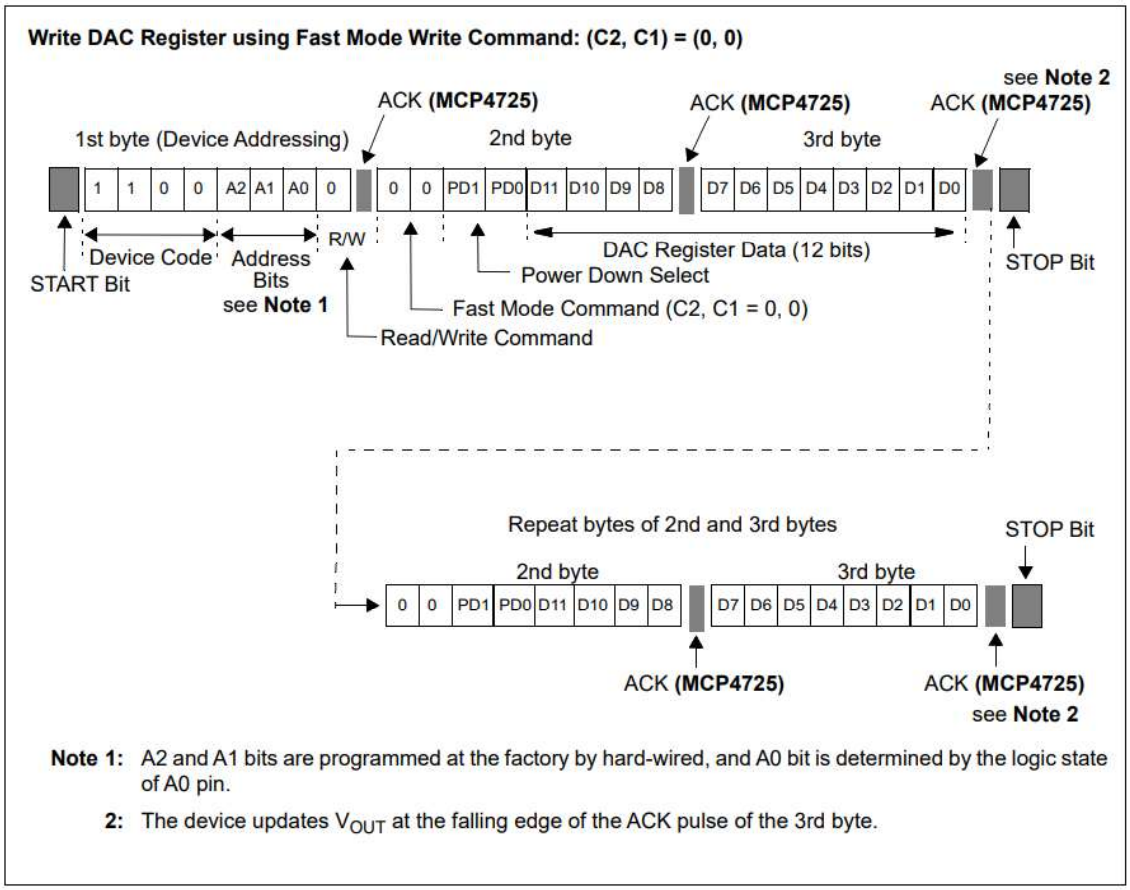


FIGURE 6-1: *Fast Mode Write Command.*

Figure 16: MCP4725 data byte configuration process for “Fast Mode”.

- Proof of Concept: This test was successful. We were able to receive output voltages at the DACs within less than 0.5% from expected values.
- Requirements Satisfied: (ER.2, ER.3, ER.4)

Voltage Translation Circuit:

Purpose:

In order to operate the varactor diodes at the desired capacitance ranges, we needed to step up our +5V source voltage to +15V in order to be able to provide the needed reverse voltages at the varactors. This value was selected as the “voltage output swing from rail” value for our selected op amp was between 2 - 4V according to the datasheet (this value was later measured, see figure 21). Assuming the worst case scenario, 15V - 4V = 11V which works well for our application. The goal was to use the +15V supply to power the LM358AN op amp in order to amplify the signals coming from the DACs which were calculated to meet the required varactor voltages. The purpose of this test was to verify that the voltage translation circuit could provide a steady output voltage to the op amp, and that the boost converter circuit worked as intended.

Additionally, it provided insight into how much power was being consumed by the DACs, microcontroller, and voltage translation circuit as well the response time of the circuit.

Setup: (see section 7.2 under hardware for detailed description of hardware setup)
Initially, the XL6009 boost converter module was used and thoroughly tested. However, after seeing the results and comparing the specifications with the MT3806, the MT3806 was used and thoroughly tested to compare to the XL6009. Note: Since the MT3806 test results far outweighed the XL6009 results, the MT3806 is the module that will be used in the final project (see pg. 39 for further details).

Each module was tested as follows:
First, a three channel power supply was used to power the boost converter module as well as provide input voltages V1 and V2 that simulate the inputs that will be provided from the output of the DACs. These values were then compared against our expected values. Once the circuit was thoroughly tested with all the values required for the varactors, the circuit was then combined with the microcontroller and DACs to verify it could provide the correct values for the varactors. The +5V supply for the voltage translation circuit was sourced from the PIC18F47K42 Curiosity Nano module. The current was measured with a multimeter in series from the +5V supply and compared to the power budget calculated value.

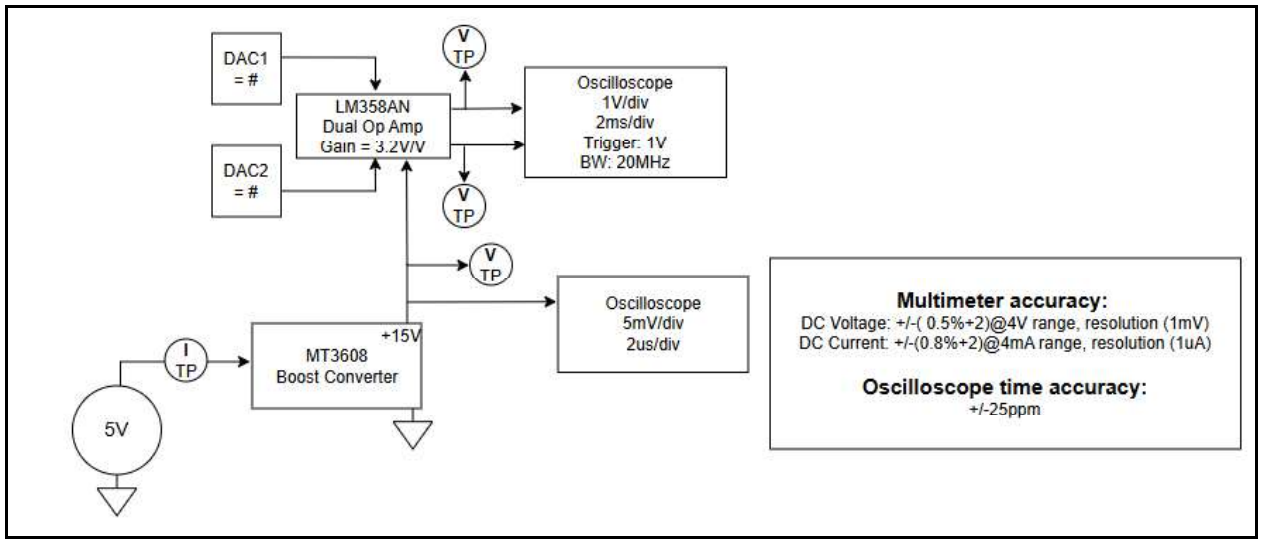


Figure 17: Circuit diagram of voltage translation circuit test setup.

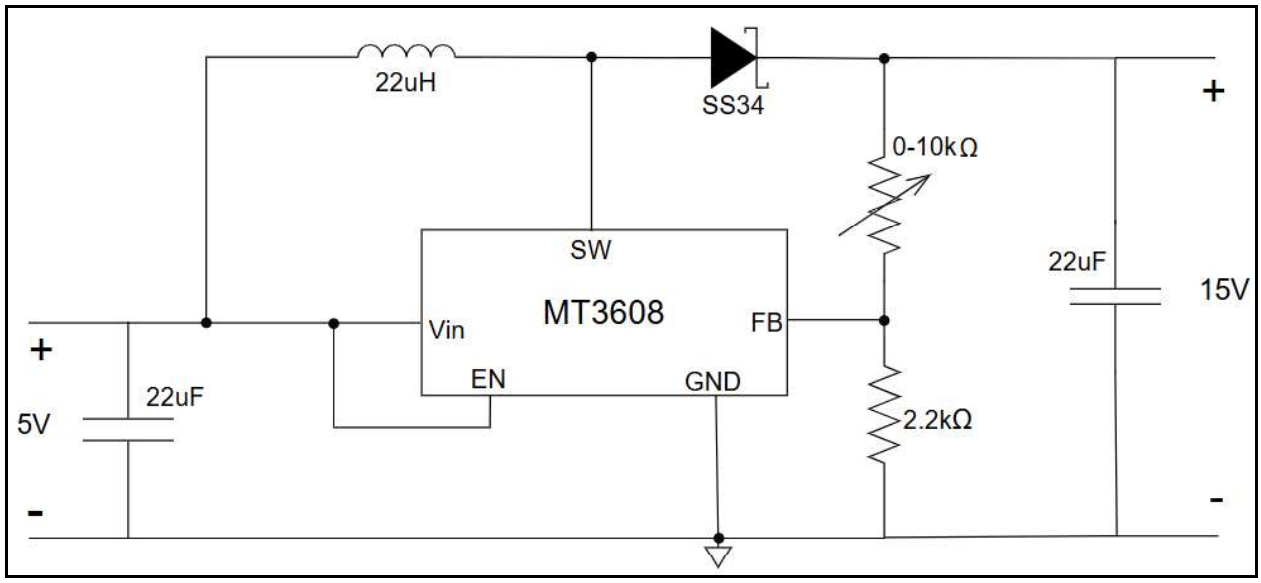


Figure 18: Circuit diagram of the Boost Converter Module shown in figure 17.

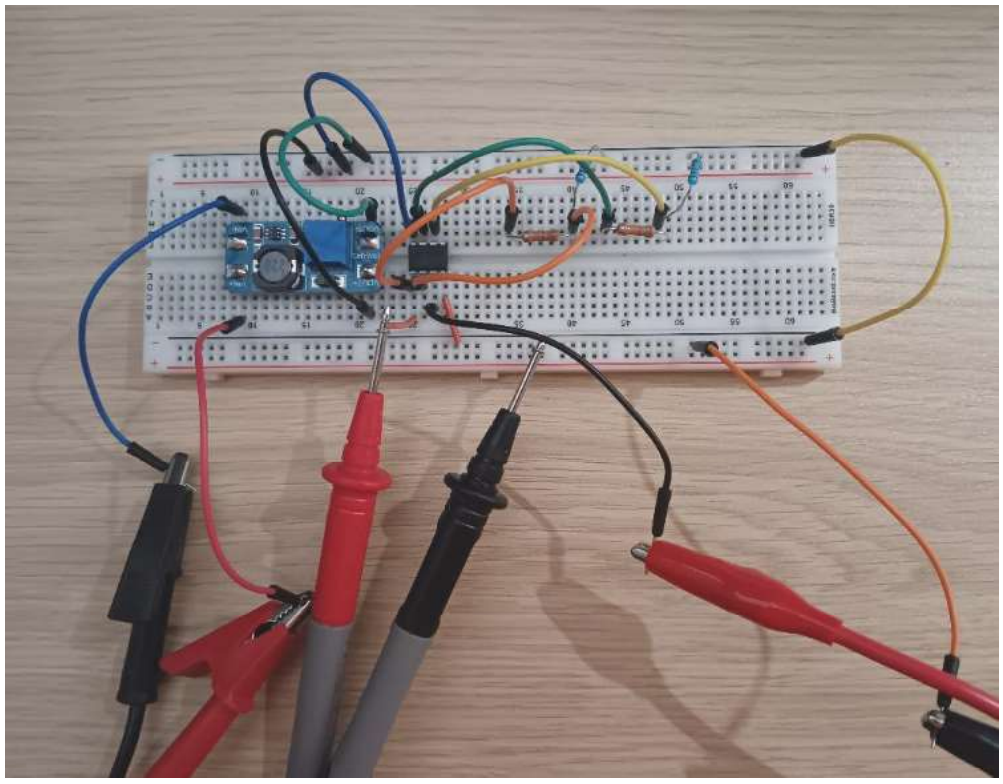


Figure 19: Physical circuit used for the first part of this test. Each op amp output was tested individually.

Var (expected)	Vin (op amp)	Var V1	Var V2	% Error Var V1	% Error Var V2
1.5	0.475	1.502	1.505	0.13	0.33
1.75	0.554	1.751	1.755	0.06	0.29
2	0.633	2.005	2.01	0.25	0.50
2.25	0.712	2.254	2.26	0.18	0.44
2.5	0.791	2.502	2.509	0.08	0.36
3	0.949	3.005	3.013	0.17	0.43
3.5	1.108	3.508	3.518	0.23	0.51
4	1.266	4.005	4.016	0.12	0.40
4.5	1.424	4.502	4.515	0.04	0.33
5	1.582	5.005	5.019	0.10	0.38
5.5	1.741	5.507	5.524	0.13	0.44
6	1.899	6.004	6.022	0.07	0.37
7	2.215	7.01	7.031	0.14	0.44
8	2.532	8.009	8.034	0.11	0.43
9	2.848	9.009	9.038	0.10	0.42
10	3.165	10.008	10.04	0.08	0.40

Figure 20: Results of measurements taken using DC power supply. The first column is the voltage we expect at each varactor. The second column is the voltage needed at each op amp non-inverting terminal input in order to obtain the expected output voltage in the first column. Columns three and four are the voltages measured at the output of each op amp. Finally, columns five and six are the error in percent from the expected output.

The LM358AN op amp was also tested to measure how much dynamic range we have as well as what the input offset voltage is. The supply was set to 10V and the other supply voltage output was fed into the non inverting terminal and varied. The max it was able to output with 10V at the positive rail was 8.78V before reaching saturation. The input to the non inverting terminal was then set to zero to measure the offset. The voltage was able to swing from a minimum of 0.1mV from negative supply rail to 1.22V from positive supply rail.

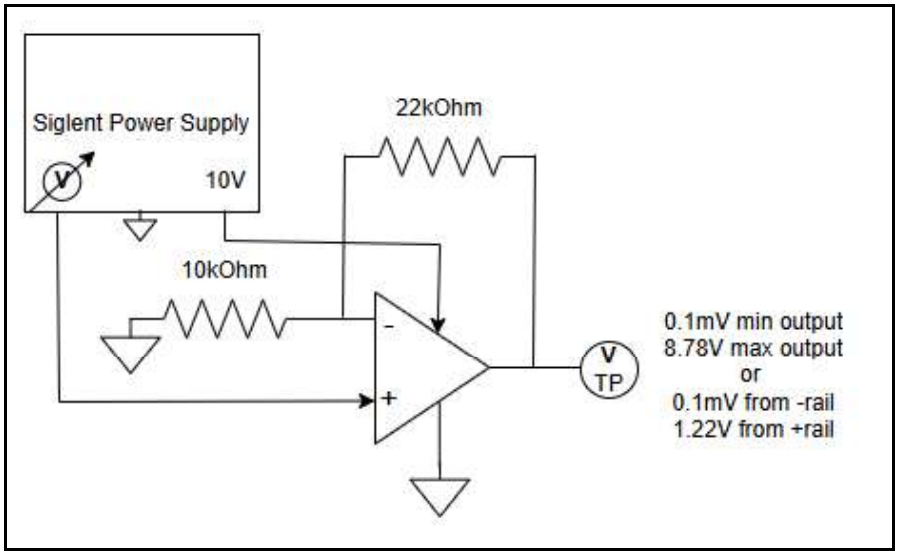


Figure 21: Test setup for measuring output voltage swing and input offset.

Testing voltage translation circuit with the DACs and microcontroller:

After combining both circuits, it became apparent that things were not working as expected. It turns out that the XL6009 boost converter module was accidentally shorted out at some point during testing, also causing the PIC18F47K42 Curiosity Nano board to become damaged as well as one of the DACs. This was apparent when the values of the DACs were not changing and were reading a constant 1.75V for each one even when the value was supposed to be 0.5V. The system was isolated and tested one component at a time starting with the boost converter module. When the boost converter module was connected to a power supply and set to a current limit up to 0.5A (similar to what a USB port would provide), the power supply was still operating in constant current mode when it should not be pulling more than 21mA under no load. The boost converter module was replaced and tested to ensure that it was operating correctly before continuing to test the other components. Additionally, the Curiosity Nano board was replaced as it was tested with only the DACs and the values stayed at 1.75V, but when swapped out with a new board, the values were updating properly. Finally the system was combined and tested for accuracy.

After further testing and research, the XL6009 boost converter module was replaced with the MT3806 module. This module was much more power efficient than the XL6009 and had a lot less noise at the output so it was used for further testing.

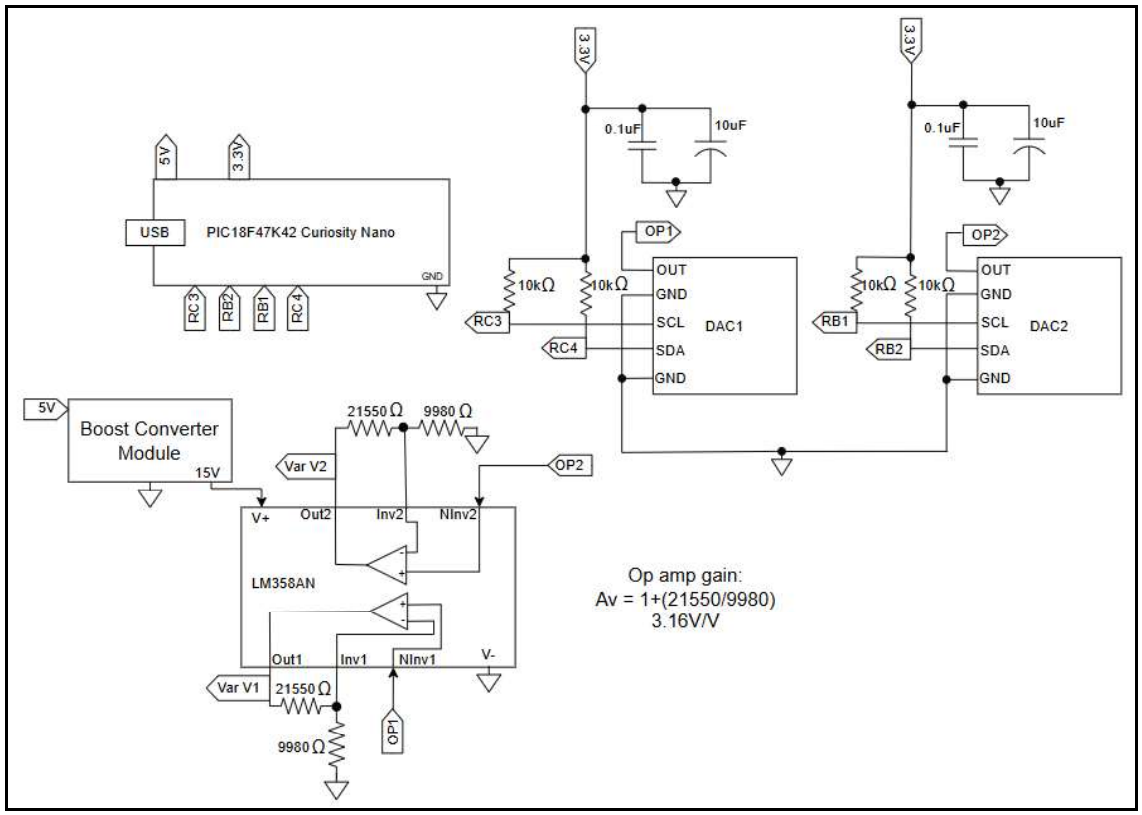


Figure 22: Combined circuit schematic.

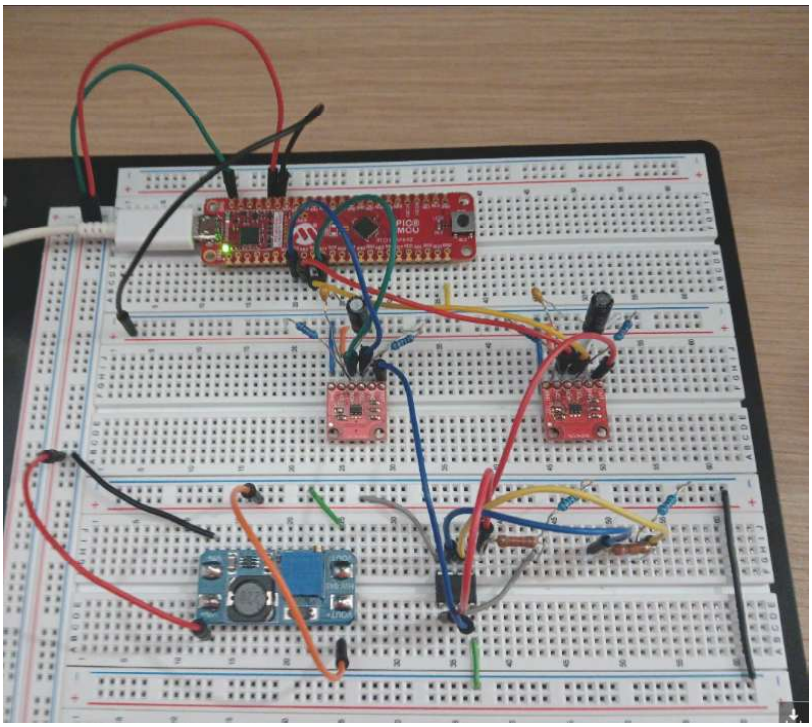


Figure 23: Physical circuit built to test the output voltages Var V1 and Var V2.

Using Complete Circuit						
Var (expected)	Vin (op amp)	DAC write value	Var V1	Var V2	% Error Var V1	% Error Var V2
1.5	0.475	589	1.493	1.499	0.47	0.07
1.75	0.554	687	1.74	1.746	0.57	0.23
2	0.633	785	1.988	1.994	0.60	0.30
2.25	0.712	884	2.24	2.244	0.44	0.27
2.5	0.791	982	2.492	2.494	0.32	0.24
3	0.949	1178	2.994	2.994	0.20	0.20
3.5	1.108	1374	3.49	3.487	0.29	0.37
4	1.266	1571	3.992	3.99	0.20	0.25
4.5	1.424	1767	4.49	4.49	0.22	0.22
5	1.582	1963	4.99	4.99	0.20	0.20
5.5	1.741	2160	5.49	5.5	0.18	0.00
6	1.899	2356	5.99	6	0.17	0.00
7	2.215	2749	7	7	0.00	0.00
8	2.532	3142	8	8.01	0.00	0.12
9	2.848	3534	8.99	9.01	0.11	0.11
10	3.165	3927	9.99	10	0.10	0.00

Figure 24: Test results for combined circuit. The circuit was able to achieve output values for the varactors within less than 1% of expected values. These values can be made even more precise should the need arise by adjusting the write value to the DACs in the code.

Dealing with noise:

There was a lot of noise being displayed on the oscilloscope when measuring the output voltage from the op amps. Most of the noise was coming from the environment since it was present even

when the scope wasn't connected to the circuit. We tried to isolate where the noise was coming from by turning off the light rail above the work bench and disconnecting other equipment powered by the same outlet. That seemed to slightly help.

Figure 25: Noise in circuit due to laptop being connected on the same power outlet.

Figure 26: Added this ferrite toroid on the power cord running to the oscilloscope, wrapping the cord three times inside it helped reduce the noise considerably.

Figure 27: Using AA batteries with ferrite toroids on the power leads to power the Curiosity Nano and adding two 470uF capacitors and one 100uF capacitor at boost module output rail we achieved a noise floor of ~5mV. We could not get it better than this.

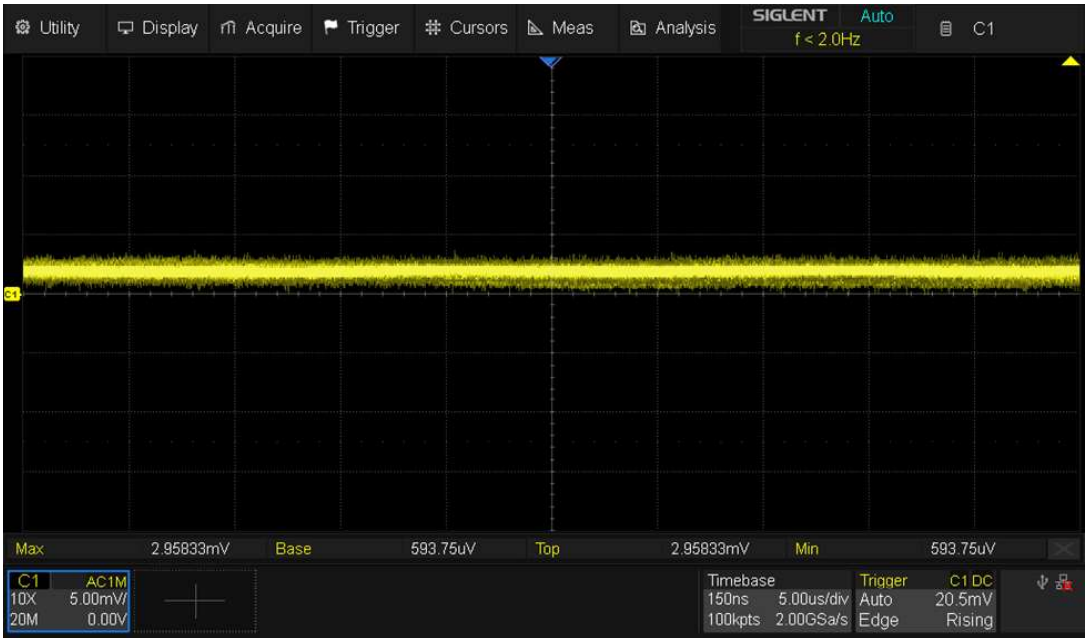


Figure 28: This became our noise floor when filtering under ideal conditions (powering circuit with clean DC supply); we could not get it lower than ~5mV.

After filtering with many capacitors at the rails and adding low pass filters to the output of each op amp, as well as decreasing the bandwidth on the scope to 20MHz (since white Gaussian noise covers all frequencies and since we are only interested in DC, we don't care to sample at higher frequencies) we were able to achieve fairly clean output signals for our varactors. However, powering the circuit through USB introduced more noise that couldn't be filtered off at this time unfortunately.

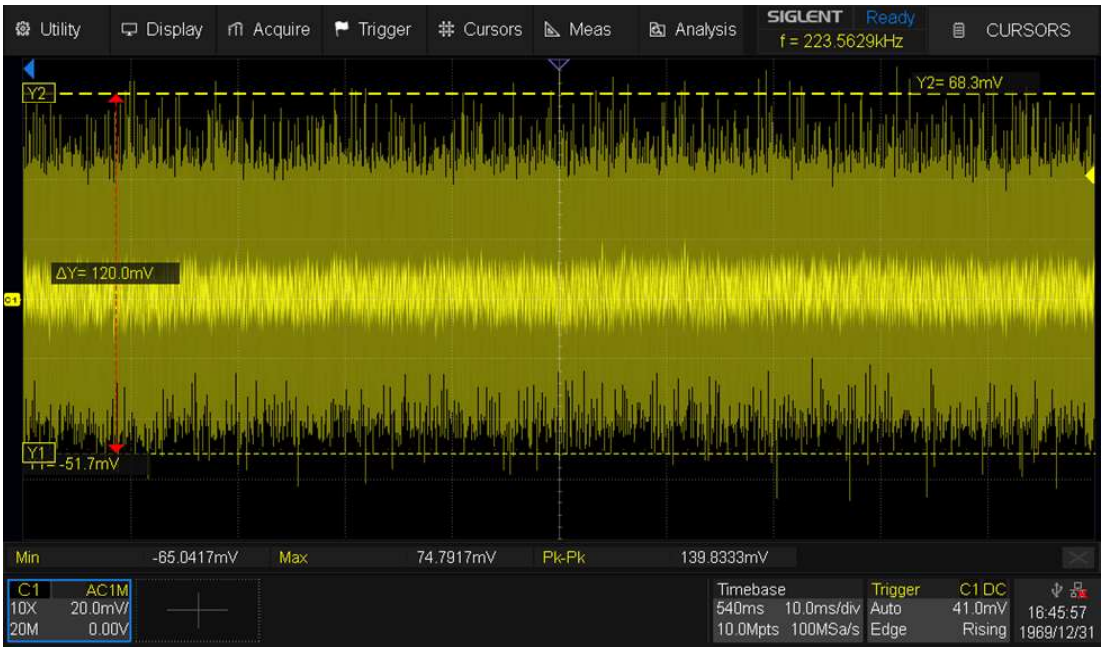


Figure 29: Boost converter output before filtering. There is 120.0mV of noise.

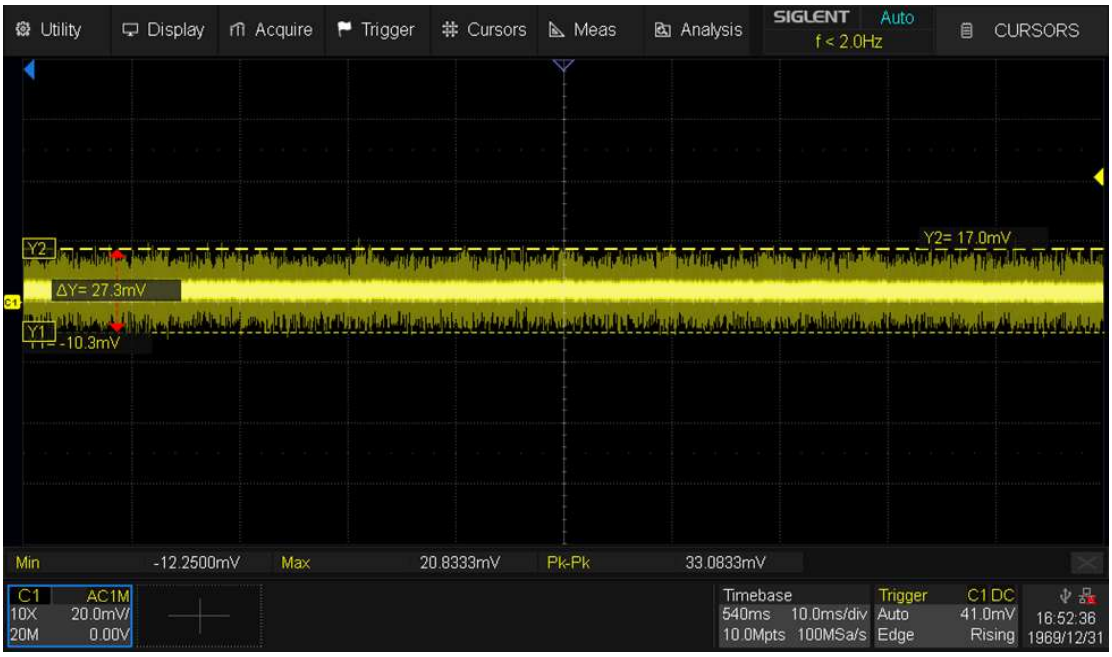


Figure 31: Boost converter output after filtering; there is 27.3mV of noise, a 23% improvement. Vertical and horizontal scales kept the same to show the difference.

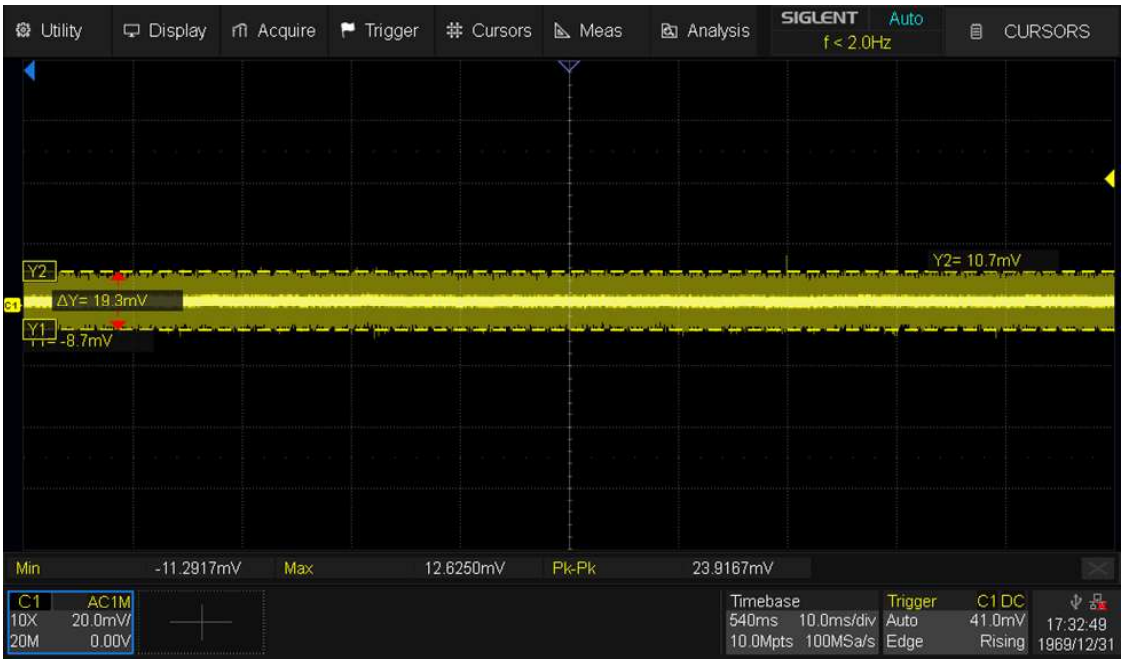


Figure 32: Noise in the circuit with probe connected to output of op amp 1 without the board powered on (Noise floor). There is 19.3mV of noise. This value will then be subtracted from the output value of op amp 1 after filtering to get total noise at output of op amp 1.

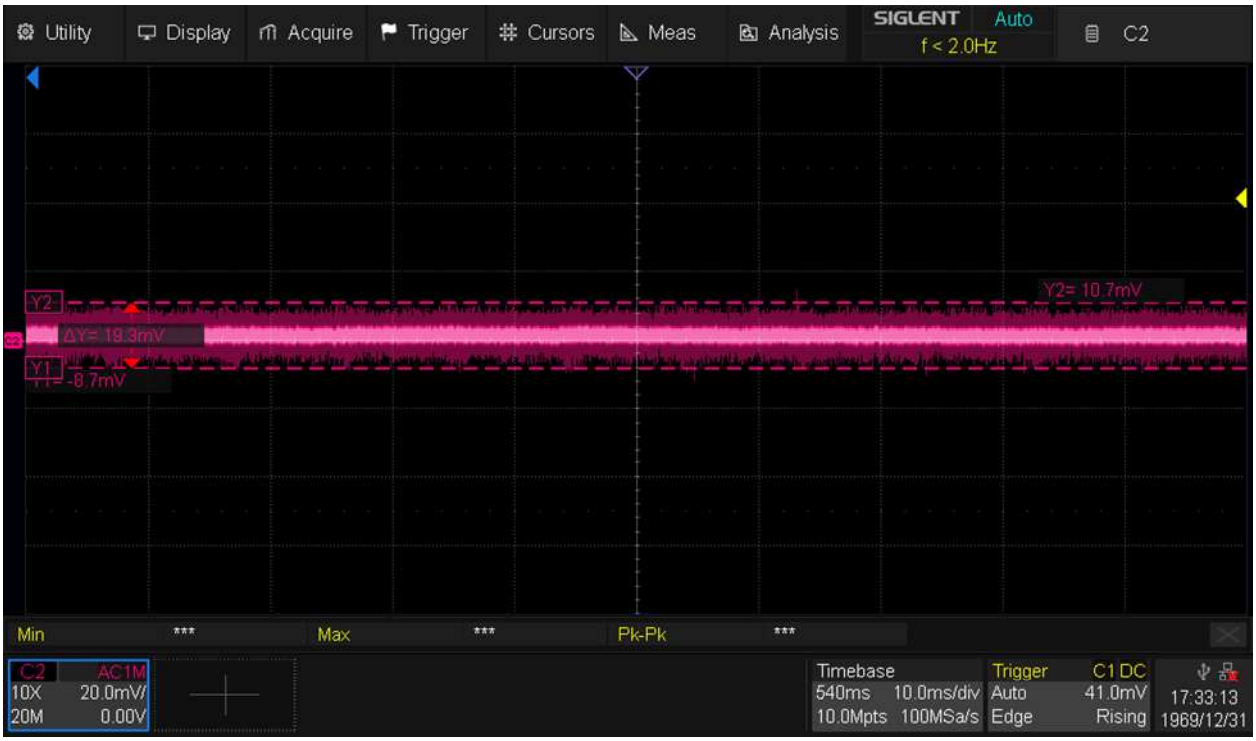


Figure 33: Noise in the circuit with probe connected to output of op amp 2 without the board powered on. This is the noise floor of the output of op amp 2. There is 19.3mV of noise.

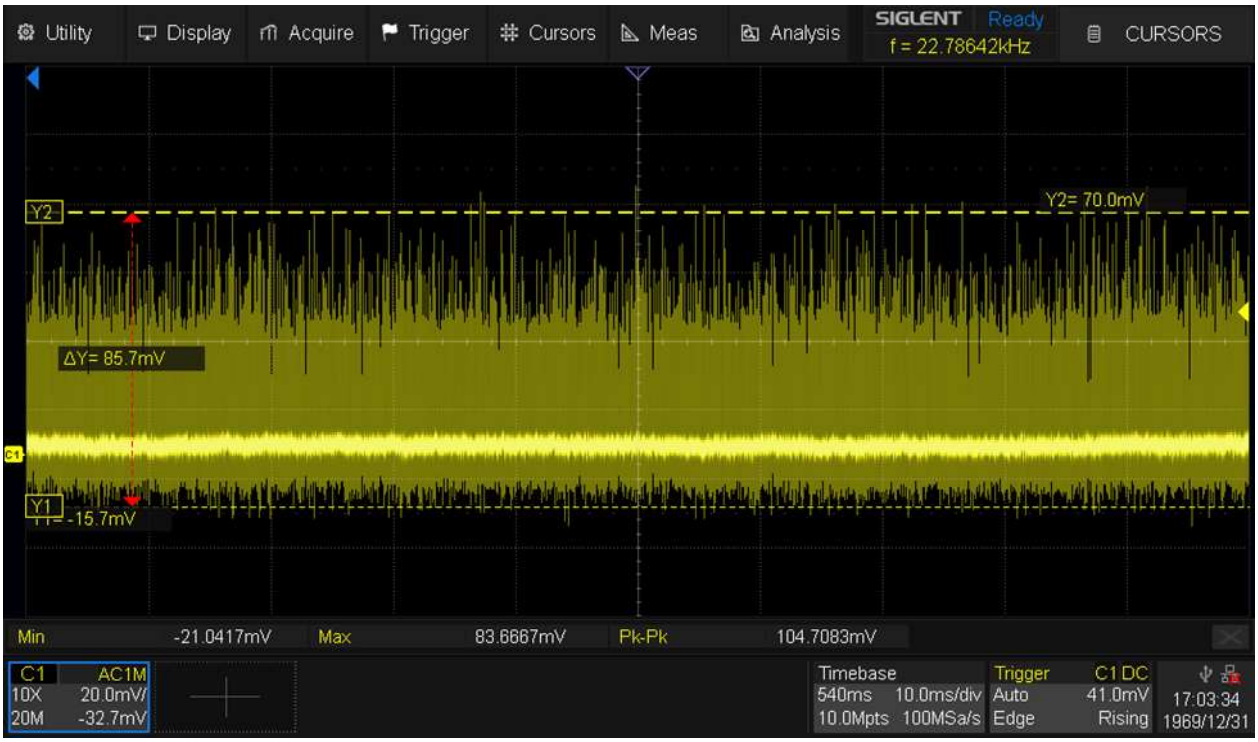


Figure 32: Output of op amp 1 before filtering. Delta Y is 85.7mV.

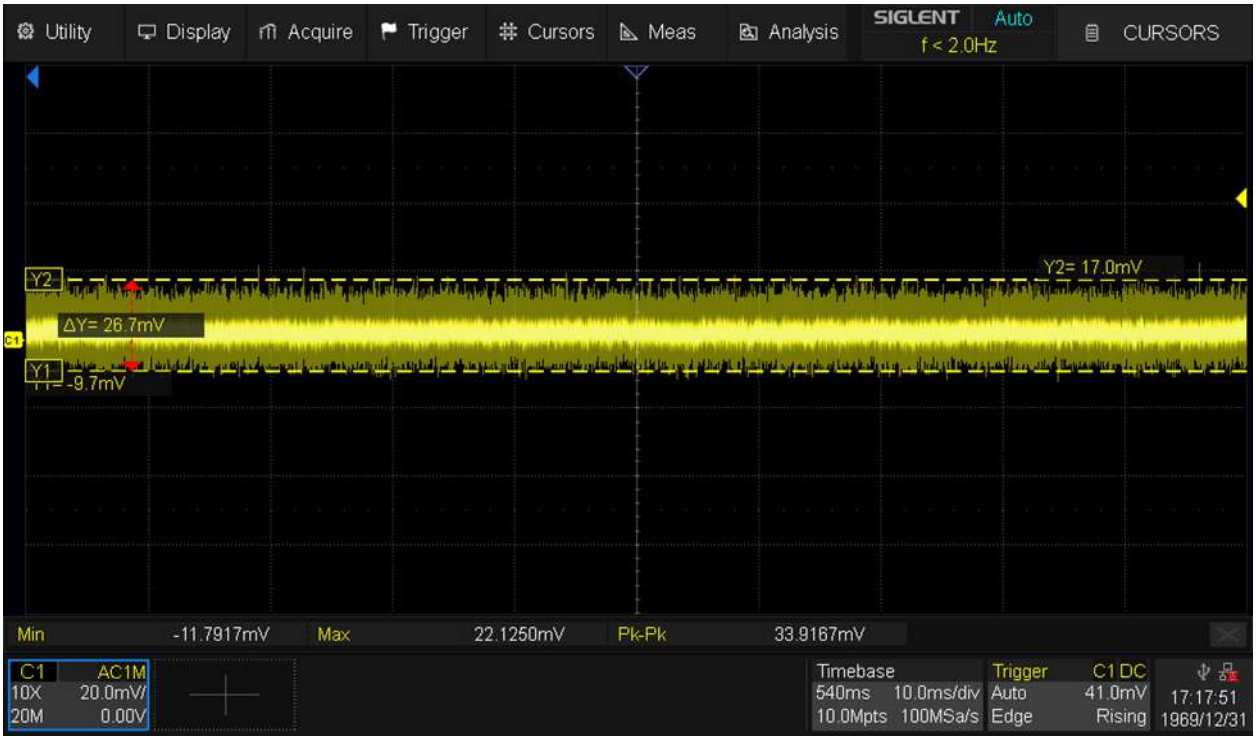


Figure 33: Output of op amp 1 after filtering. Total noise out of op amp 1 is 26.7mV - 19.3mV = 7.4mV. This is a 31% improvement.

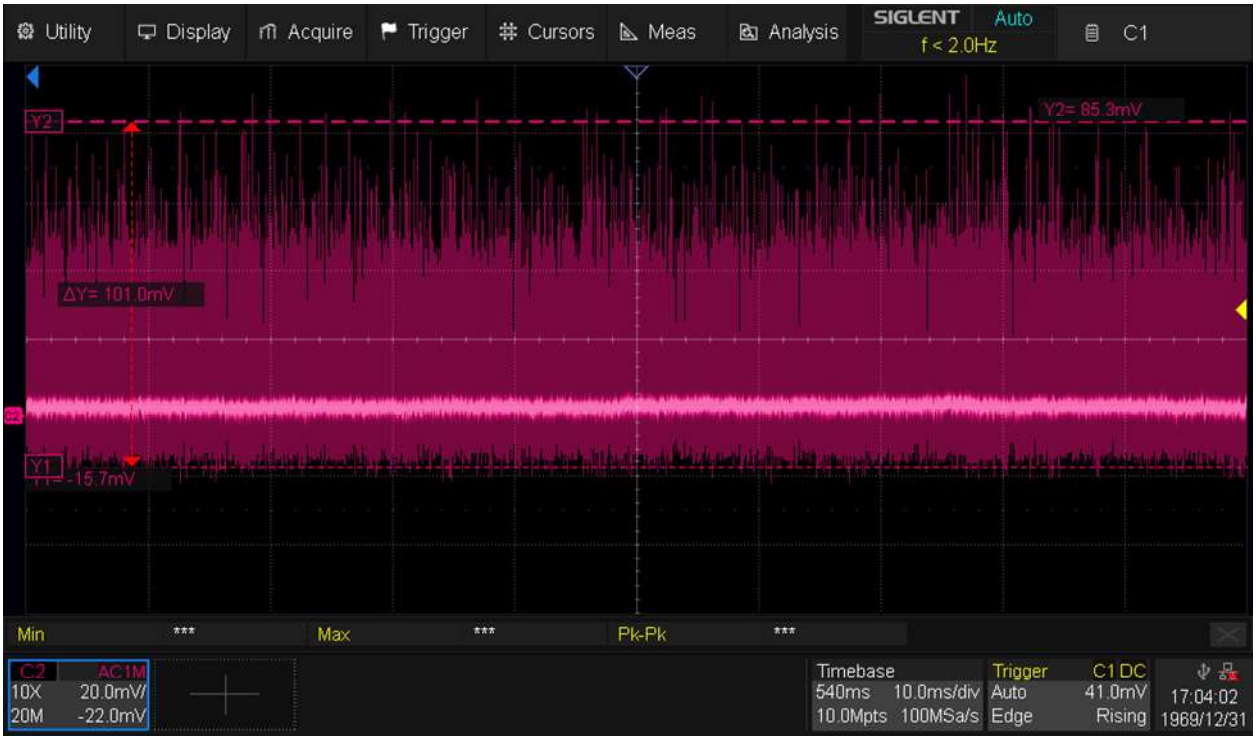


Figure 34: Output of op amp 2 before filtering.

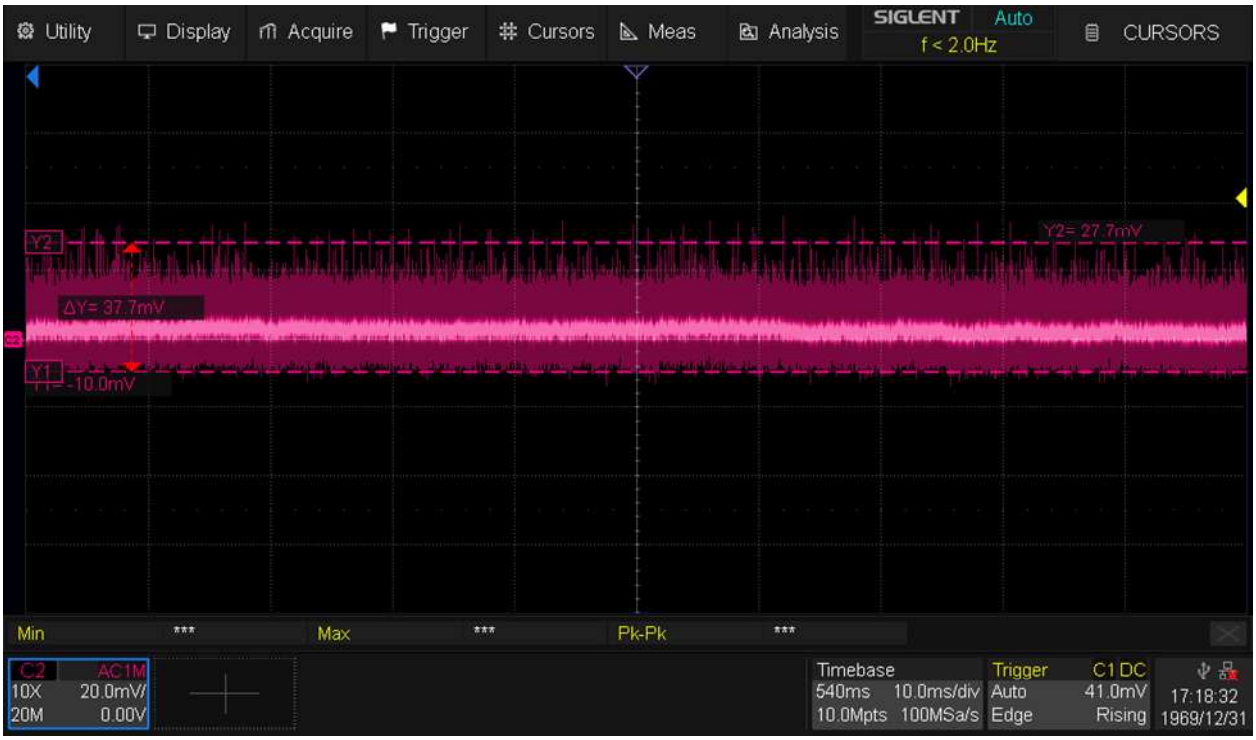


Figure 35: Output of op amp 2 after filtering. Total noise out of op amp 2 is 37.7mV - 19.3mV = 18.4mV. This is a 37% improvement.

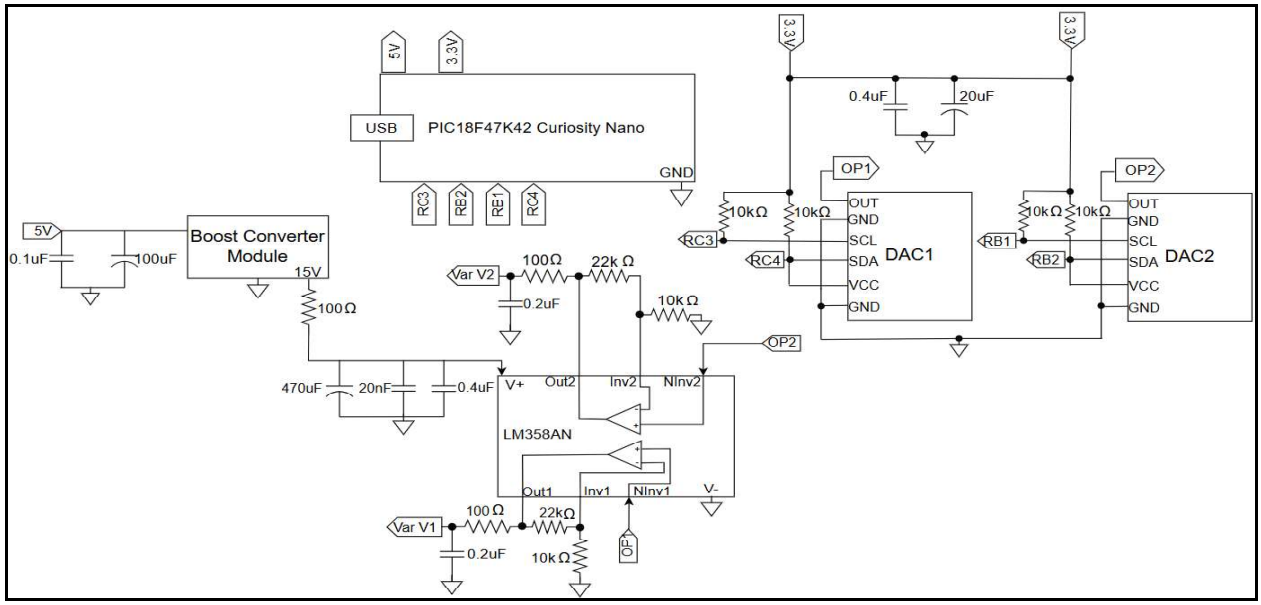


Figure 36: New circuit schematic for combined circuit.

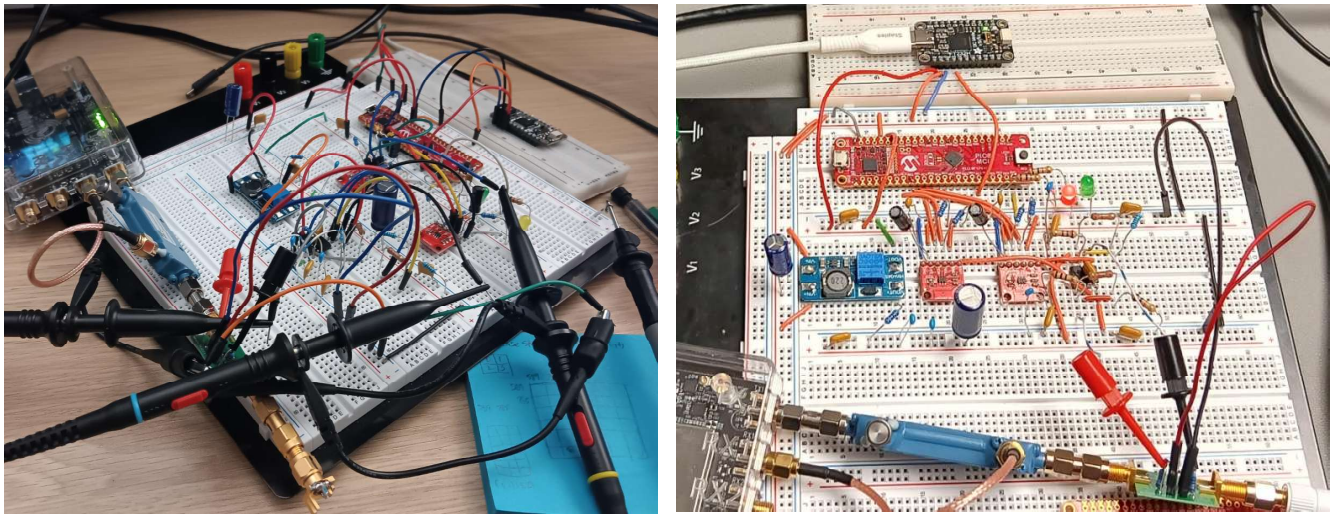


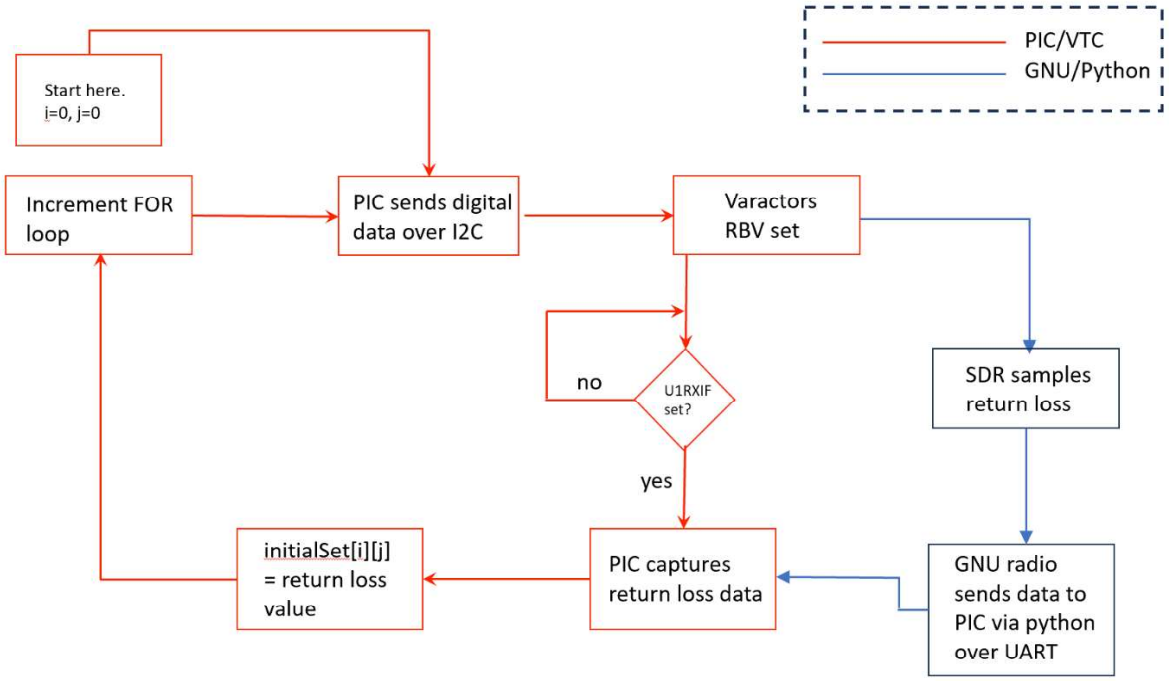
Figure 37: Cleaning up the circuit a bit to help stabilize the outputs from fluctuating. This helped with noise reduction considerably.

- Results: The circuit worked really well. This should give us a good starting point, and adjustments can be made to op amp input values later on to compensate for the error if need be.
- Proof of Concept: This test was successful. We were able to receive expected output voltages at the op amp within less than 1% of expected value.
- Requirements Satisfied: (ER.2, ER.4)

Testing of the Microcontroller Algorithm:

Purpose: Demonstrating the functionality of the matching network hardware was a crucial step towards our project's goal, but our engineering requirements state that the matching process must be accomplished automatically without input from the end user. This requires an embedded microcontroller that executes a custom algorithm to find the best possible match for a variety of potential environments.

Setup: The algorithm we chose to implement used a coarse-to-fine methodology that attempts several combinations of voltages for each varactor and then hones in on the best possible match. The structure is quite simple; each varactor can assume 30 discrete voltages that can be spaced apart at the programmer's discretion. The algorithm initially samples 10 out of the 30 voltages for each varactor and relates the return loss received by the SDR with each voltage combination. From there, it finds the combination of voltages that gave the highest return loss and repeats the process but with a narrower scope. This allows the algorithm to always find the best possible match. A general flowchart of the communication between the MCU and SDR is show below.



In our testing, we found that voltages beyond 5.7 V showed diminishing returns, which is why each varactor can be tuned from 0 to 5.7 V.

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
V1	0	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1	1.2	1.4	1.6	1.8	2	2.2	2.4	2.6	2.8	3	3.3	3.6	3.9	4.2	4.5	4.8	5.1	5.4	5.7
V2	0	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1	1.2	1.4	1.6	1.8	2	2.2	2.4	2.6	2.8	3	3.3	3.6	3.9	4.2	4.5	4.8	5.1	5.4	5.7

Notice the highlighted voltages for varactors 1 and 2. These are the values which will be sampled by the algorithm during the coarse phase of the search - 10 combinations of voltages that will each have a return loss associated with it and stored in a 10x10 array.

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
V1	0	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1	1.2	1.4	1.6	1.8	2	2.2	2.4	2.6	2.8	3	3.3	3.6	3.9	4.2	4.5	4.8	5.1	5.4	5.7
V2	0	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1	1.2	1.4	1.6	1.8	2	2.2	2.4	2.6	2.8	3	3.3	3.6	3.9	4.2	4.5	4.8	5.1	5.4	5.7

In the figure above, consider the case where the best match during the coarse search was with varactor 1 biased to 0.3 volts and varactor 2 biased to 0.9 volts. In that case, the “fine-tuning” phase would search through all available voltage combinations that were initially excluded, as shown below.

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
V1	0	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1	1.2	1.4	1.6	1.8	2	2.2	2.4	2.6	2.8	3	3.3	3.6	3.9	4.2	4.5	4.8	5.1	5.4	5.7
V2	0	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1	1.2	1.4	1.6	1.8	2	2.2	2.4	2.6	2.8	3	3.3	3.6	3.9	4.2	4.5	4.8	5.1	5.4	5.7

Ultimately, we found that this approach finds an acceptable match within a reasonable timframe of 772ms. While not quite ideal, limitations within GNU radio and the python scripts used to transmit data over UART limit the response time.

- Results: Successful match within 772ms.

- Proof of Concept: Was able to use an oscilloscope to verify the matching time and observed feedback from GNU radio to ensure the return loss was was at least 20dB.

- Requirements Satisfied: (ER.1, ER.3)

Testing SDR Can Measure Return Loss:

Purpose:

The purpose of this test was to verify that the SDR can output a value for return loss that is reasonably close to the value returned from a calibrated source for the same load. A Keysight FieldFox will be used as the calibrated source.

Setup:

For this test, we used seven different loads and had the SDR read out the return loss value for each load. We then connected each load to the Keysight Fieldfox (N9918A) after doing a full two port calibration and again read the return loss value for each load. We then compared the two values to get an idea of how accurate the SDR readings for return loss are.

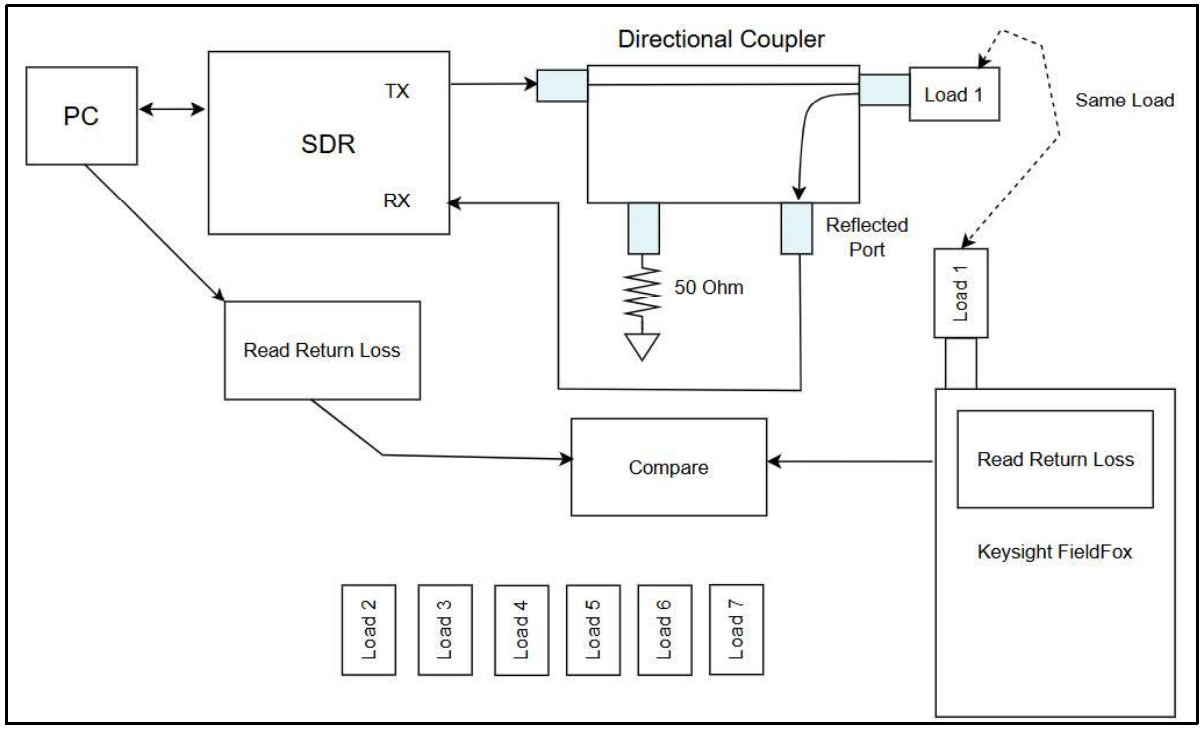


Figure 38: Block diagram showing setup for testing SDR accuracy.

- <u>Results:</u>

Return Loss Comparison			
Load #	Cal. Source(dB)	GR(dB)	Diff. (dB)
1	2.367	2.350	-0.017
2	4.513	6.996	2.483
3	8.313	9.259	0.946
4	0.915	1.234	0.319
5	1.418	4.379	2.961
6	2.686	6.032	3.346
7	8.932	6.603	-2.329

Figure 39: This table shows the comparison between the readings from the SDR (labeled GR(dB)) and the Fieldfox (labeled Cal. Source(dB)). The difference in the worst case was 3.346dB off. This value is substantial. We were not quite sure where the discrepancy was coming from.

- Proof of Concept: Although the values were off by quite a bit, GnuRadio was still reporting a return loss of around 25dB when it was matched. GnuRadio is set up with a threshold value of 25dB because the noise floor was at around 27-28dB. Therefore, any value of return loss greater than 25dB is capped at 25dB, so theoretically, the return loss could be a slightly higher value.

- Requirements Satisfied: (ER.1, ER.5)

Power Consumption:

Purpose:

When measuring the total power consumption of our device and determining an ideal power consumption target value, we focused on ensuring efficient operation while maintaining the performance requirements of the system. We then performed a couple tests to obtain a practical application value and compare the value with our projected power consumption from our power budget. The power budget has changed since last semester's estimate as some of the components have been changed. It is now much lower than we initially anticipated.

Setup:

We first developed a power budget by reviewing the datasheets of the components we used and calculated the total power consumption. The power consumption of each component was also measured individually and then measured as a whole when the project was complete.

Power Budget	
Component	Power Consumption (mW)
FT232H	126
PIC18F47K42	60
MCP4725 (x2)	2.64
LM358	30
Boost Converter (under load)	105
Total	323.64

Figure 40: Power consumption of each component based on the information from each component's datasheet.

To measure the total power, we used a USB tester breakout module that allowed us to insert our ammeter in series with the device, as well as measure the voltage from the USB port.

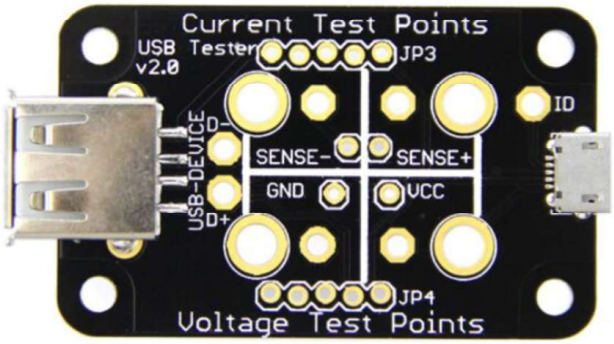


Figure 41: USB tester breakout board used to measure the voltage and current being pulled from the USB port.

The DACs were then set using a simple code to output the maximum voltage they are capable of handling (a DAC write # of 4095). This gave us the maximum amount of power that would be drawn from the circuit.

- Results: The voltage at the USB port was measured as 5.10V. The total current drawn was measured as 84mA, for a total power of 428mW.
- Proof of Concept: This test was successful. Our device had a power consumption of less than 700mW.
- Requirements Satisfied: (ER.2)

1. Ethics of the Engineering Profession and Our Project (Must be 0.5 page)

Ethical design in engineering involves considering the impacts on the environment, society, and on individuals when designing new products [5]. While the components in our design are not sustainable, we have done our best to minimize the environmental impact. By using USB power instead of using disposable or rechargeable batteries, our project reduces the reliance on materials like lithium and cobalt, which have a negative environmental impact through their extraction and disposal [6]. Unfortunately, our device does not incorporate a modular design approach, which limits the potential for device repair and reusability after the end of its lifecycle.

Our device contributes positively to society by helping devices last longer and reduce interference. By adaptively matching the antenna impedance, the device decreases reflected power levels, which enhances the efficiency and lifespan of connected devices. This not only reduces the energy consumption of these devices but also minimizes the risk of damage to components caused by high levels of reflected power. The longer a device lasts, the less frequent it ends up as e-waste.

Finally, our device is no more harmful than existing wireless devices and introduces key benefits that outweigh its minimal environmental footprint.

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